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1974
N00014-74-C-0020
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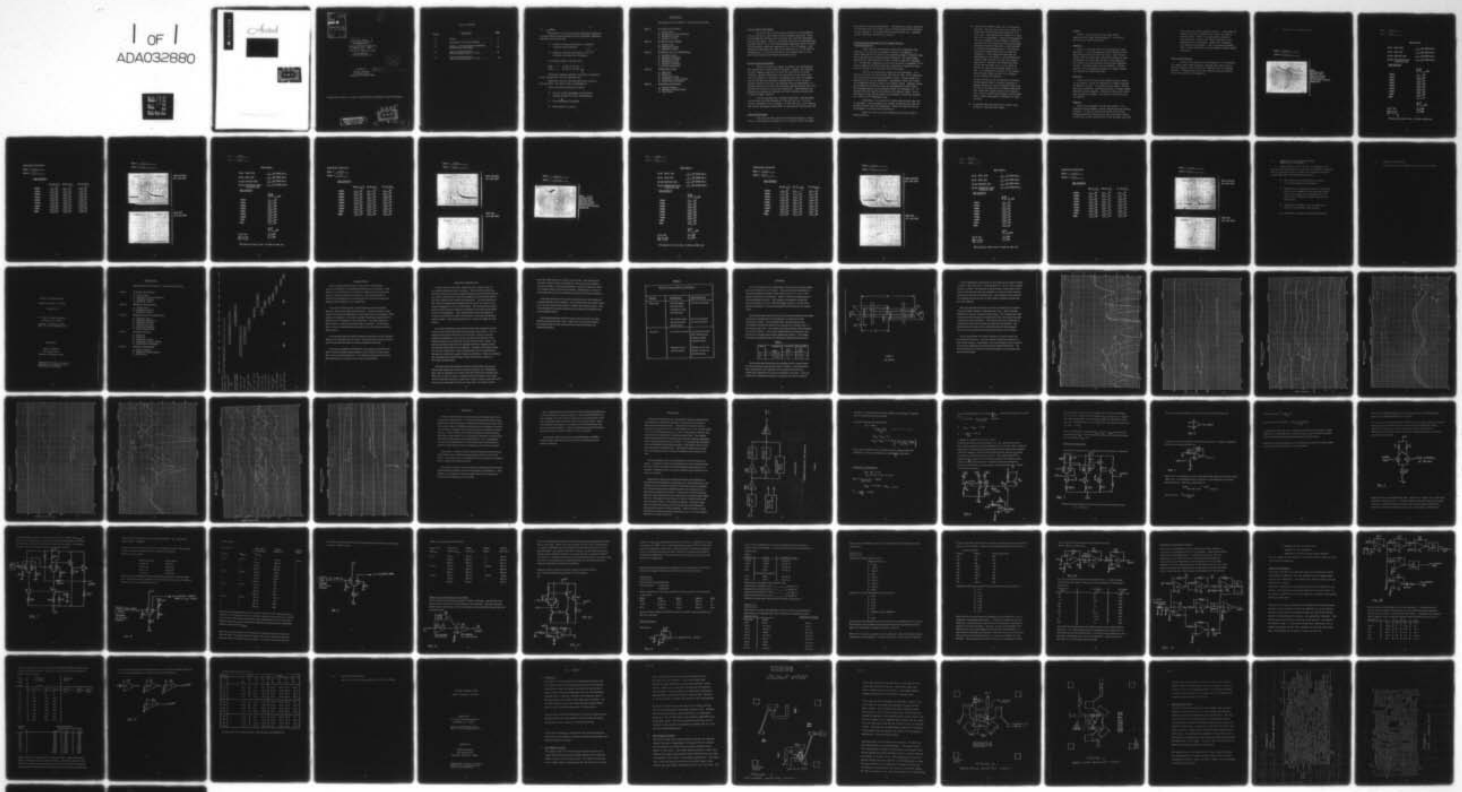

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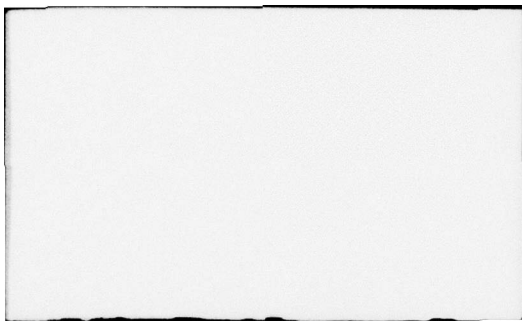

(1)

(6) FINAL REPORT

Prepared For

U.S. Naval Research Laboratory
Washington, D.C. 20375

Contract No. N00014-74-C-0020

Requisition No.
00173-3-006371/2-27-73

(11) 1974
(12) 82 p.

Prepared by

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(15) N00014-74-C-0020

S/C - B 392640

TABLE OF CONTENTS

1.0 SUMMARY

The objective of this Research and Development program was to develop Direct Coupled Microwave Detector Logarithmic Amplifiers packaged in one housing with:

1) Detector circuitry fabricated on a substrate using Thin Film Techniques.

2) Amplifier circuitry fabricated on a 1" x 1" substrate using Thick Film Techniques.

Two frequency bands of interest were:

Band I – 2.6 GHz to 8.0 GHz, and
Band II – 6.9 GHz to 18.0 GHz.

Deliverable hardware consisted of one pair of matched detector log amplifiers for each frequency band.

Program was laid out with five major tasks, which are described below. For details refer to Paragraph 4.0.

Three tasks were simultaneously started.

1) Critical circuit development using discrete packaged integrated circuits and components.

2) Microwave coupler development.

3) Hybridization of circuits.

MAJOR TASKS

NRL DEVELOPMENT PROGRAM - Integrated Det-Log Amp

TASK 01 LOG AMP DEVELOPMENT

a. Design Labor
b. Breadboard Circuit Fabrication
c. Breadboard Testing
d. Substrate Testing

TASK 02 DETECTOR DEVELOPMENT

a. Design Labor
b. Breadboard Testing
c. Substrate Testing

TASK 03 SUBSTRATE LAYOUT & FABRICATION

a. Substrate Layout
b. Substrate Fabrication
c. Mechanical Design
d. Fabricate Housing
e. Composite Assembly
f. Process Engineering

TASK 04 INTEGRATION TASKS

a. Write ATP
b. Write QTP
c. Composite Testing
d. Acceptance & Qual. Testing
e. Environment lab Charges

TASK 05 PROGRAM MANAGEMENT

a. Program Planning
b. Quarterly Progress Reports
c. Final Report

Critical Circuit Development

One of the most critical circuit sub-block in this program was a very low DC drift, ultra-stable and wide bandwidth gain block. Three to four different techniques were tried with very extensive experimentation and data taking. Finally, a successful gain block was developed which featured a gain of 35 to 40 dB with bandwidth capability from DC to 50 MHz. DC drift without temperature compensation was 2.0 u v/^{o}C maximum. With temperature compensation the drift can be reduced to 0.2 u v/^{o}C (refer to Paragraph 4.0). It should be pointed out that normally there is 50 to 60 dB linear amplification before logarithmic process.

Microwave Coupler Development

The first iteration in coupler development was interdigitated type fabricated on alumina metalized substrate. Couplers were designed to cover frequency range from 2.6 to 8.0 GHz and from 6.9 to 18 GHz. Initially, signicant difficulties were experienced in the actual realization of couplers on substrates. Performance data (refer to Paragraph 4.0) for S/C band unit exhibited a maximum VSWR of 1.33 to 1.0 and a minimum isolation of 20.0 dB. The coupling value was approximately 3.3 dB except for the lower end of the band where coupling was much worse than expected in the order 5.0 dB for the coupled port. Specifications were planned to be improved by improving line width resolution and gap width to achieve tighter coupling.

For the C/Ku band unit, (detailed performance, refer Paragraph 4.0) the worst case VSWR occurred at 14 GHz and was 2.6:1. This was directly attributed to poor stitching. In this case also, it was expected that circuit performance would improve by adjusting the line and gap width.

Hybridization Attempt

While the low drift gain block was being developed at circuits level, it was decided to fabricate on 1" x ½" substrate three log stages

along with the final summing amplifier. The purpose was to get a practical feel for the results for a known circuit sub-block using hybrid integrated circuit techniques. After some difficulty with bonding, etc., comparable results to descrete sub-block were achieved.

Overall Circuits Development for the Complete Detector Logarithmic Amplifier

After achieving satisfactory results with a high gain linear amplifier, it was decided to breadboard a detector log amplifier. A tunnel diode detector was used for the simulation purpose as Schottky diodes and 3.0 dB hybrids were being evaluated separately. The block diagram configured for implementation of a DLVA is shown in Figure 17, Paragraph 4.0. A temperature compensation circuit also described in Paragraph 4.0 was used to compensate the drift from linear amplifiers by applying an equal amount of voltage to the non-signal side of log stages.

The unit was successfully aligned at room temperature. It resulted in less than ±1.0 dB linearity from TSS to 0 dBm. First temperature run on the circuit gave quite unacceptable results. Various stages were separated and re-run over temperature. Unacceptable results were traced to two amplifiers placed in shunt at the detector output. Impedance change and interaction was the main reason for nonrepeatable DC drift results. Block diagram approach was reconfigured (Figure 18, Paragraph 4.0). Essentially only one amplifier was placed at the detector output. The experiment was re-run and satisfactory and acceptable results were obtained over -54°C to +75°C temperature range.

Furthermore, it was decided to confirm that low drift gain cell is repeatable. For this purpose, two complete breadboards were made and extensive results taken over temperature. Results are shown at the end of Paragraph 4.0 and were quite satisfactory.

After this stage a two prong program was initiated, which is summarized below:

1) Evaluation of Schottky diodes for DC tracking and matching. For this test several test circuits were built where Schottky diodes were bonded 10 to 15 mils apart. Each package had 10 diodes in it, packaged in a 24 pin package. Extensive experimentation was done on several of these packages. Basically, packages were first subjected to non-operating high temperature bake and temperature cycling followed by 168 hours of operating burn-in. The above was followed by detailed data taking over time and temperature. After running the experiment for approximately 2 to 3 months, it was concluded that Schottky diodes could not be used in DC coupled applications. The worst case differential drift between any two diodes was 4 to 5 mv, which restricts the useful low end dynamic range to -20 dBm. As a conclusion of the above it was mutually agreed between Aertech and NRL to use packaged co-axial tunnel diode detectors.

   At the same time, it was also decided to terminate the development effort on couplers, primarily as changes made did not result in expected results and also due to the fact that use of tunnel diode detectors implied that couplers would not be required. This is true as tunnel diode detectors give low VSWR even at 0 dBm, when properly terminated into video circuitry.

2) An approach where hybridization of circuits would proceed in a parallel mode, namely:

Hybrid I

Hybrid I consisted of three log stages, power supplies and the output summing amplifier. Two circuits were built and successfully tested.

Hybrid II

Hybrid II consisted of two low drift high gain linear amplifiers. It also had appropriate level shifting circuits and interface circuits for the log stages. After initial trouble shooting satisfactory results were achieved in terms of bandwidth, rise time, gain and pulse swing capability. Two circuits were then subjected to burn-in and temperature cycling. Acceptable results were not achieved. Probable cause for poor temperature performance was improper thermal distribution and intermittent bonds.

Hybrid III

Work on Hybrid III was started before testing on Hybrid II was complete. Hybrid III consisted of a complete logarithmic amplifier circuit. It included five log stages, two high gain linear amplifiers, inverting amplifiers, an output summing amplifier and power supplies. However, all the circuit blocks were externally accessible. The results of this hybrid were satisfactory.

Hybrid IV

Hybrid IV was planned to be the Final Format. It included some design changes, internal frequency and gain setting resistors. In order to increase the yield, critical gain setting and offset setting resistors were "chip type" instead of thick film printed resistors most of the resistors (over 100)

were printed using three different screens. A large number of different screens were needed due to a very wide range of resistor values. Hybrid IV was successfully aligned at room temperature. However, its thermal stability at room temperature was not acceptable. Results over temperature were completely unacceptable. Most of the thermal problems, after a careful examination, were attributed to uneven thermal distriubtion.

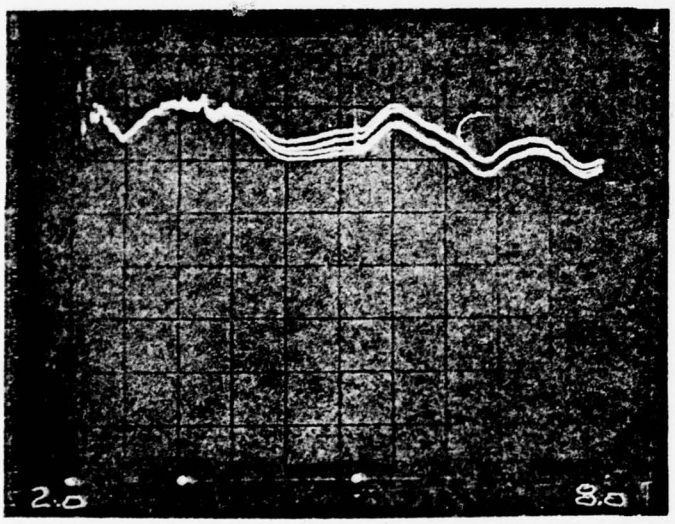
Final Circuit Iteration

Circuits were relaid out on four different 1" x ½" substrates. For example, power supply regulators (dissipate most heat) were on a separate substrate and low drift linear amplifiers were on a separate substrate. Extremely good results were achieved using this approach. Results are discussed in Paragraph 2.0.

2.0 PERFORMANCE OF DELIVERED HARDWARE

MODEL # LDX1002

SERIAL # 16357-58



MODEL
DETECTORS USED
SELECTED FROM
THE FOUR MATCHED
DETECTORS SHOWN
IN THE SWEPT RESPONSE
PHOTOGRAPH

MODEL # LDX1002

SERIAL # 16357

TEST RESULTS

(3.8)	DELAY TIME	25 nS (80nS max.)
(3.9)	RISE TIME	30 nS (80nS max.)
(3.10)	SETTLING TIME	70 nS (80nS max.)
(3.11)	PROPOGATION DELAY + SETTLING TIME	95 nS (140nS max.)

LOG LINEARITY

	(4.6) OP AT ____ GHz
-40dBm	233 mV
-35dBm	619 mV
-30dBm	1003 mV
-25dBm	1436 mV
-20dBm	1866 mV
-15dBm	2297 mV
-10dBm	2670 mV
-5dBm	3042 mV
0dBm	3447 mV

	(4.6) at ____ GHz
(4.2) TSS	41.5 dBm
TSS at 5MHz B.W. (4.3)	43.2 dBm

TSS should be better than -41.5dBm at 5MHz B.W.

TEMPERATURE PERFORMANCE

MODEL # LDX1002

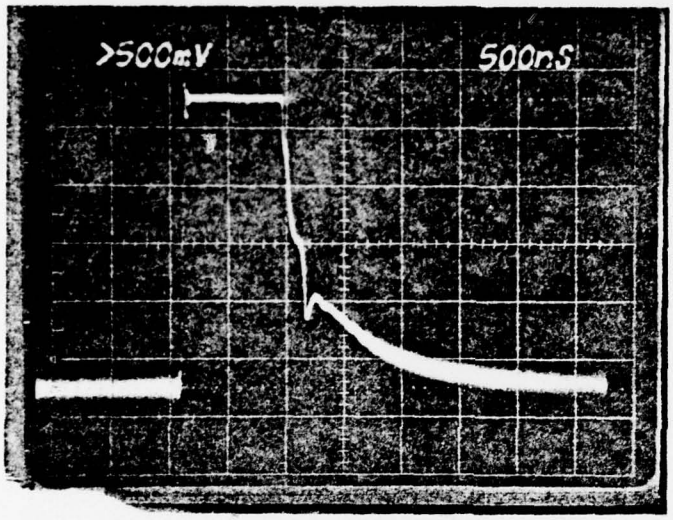
SERIAL # 16357

LOG LINEARITY

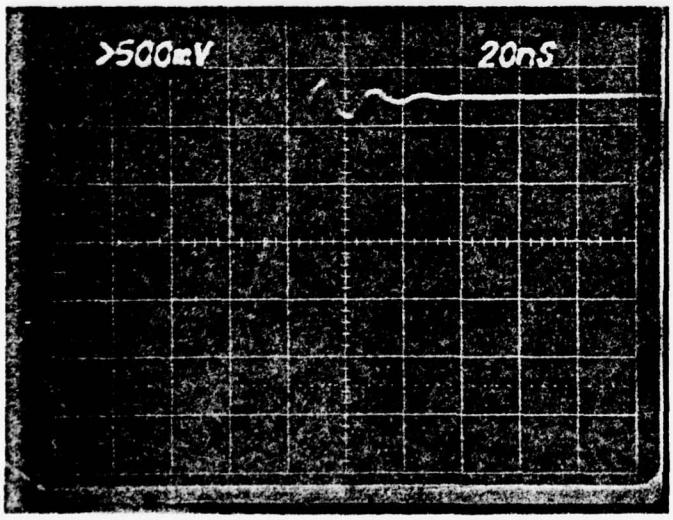
	OP AT +25°C	OP AT -54°C	OP AT +85°C
-40dBm	233 mV	156 mV	256 mV
-35dBm	619 mV	500 mV	614 mV
-30dBm	1003 mV	950 mV	1014 mV
-25dBm	1436 mV	1380 mV	1432 mV
-20dBm	1866 mV	1769 mV	1846 mV
-15dBm	2297 mV	2141 mV	2282 mV
-10dBm	2670 mV	2536 mV	2658 mV
-5dBm	3042 mV	2910 mV	3012 mV
0dBm	3447 mV	3307 mV	3433 mV

MODEL # LDX1002

SERIAL # 16357



PULSE RESPONSE
AT 0 dBM INPUT



RISE TIME
AT 0 dBM INPUT

MODEL # LDX1002

SERIAL # 16358

TEST RESULTS

(3.8)	DELAY TIME	25 nS (80nS max.)
(3.9)	RISE TIME	25 nS (80nS max.)
(3.10)	SETTLING TIME	60 nS (80nS max.)
(3.11)	PROPOGATION DELAY + SETTLING TIME	85 nS (140nS max.)

LOG LINEARITY

	(4.6) OP AT ____ GHz
-40dBm	253 mV
-35dBm	600 mV
-30dBm	982 mV
-25dBm	1406 mV
-20dBm	1830 mV
-15dBm	2237 mV
-10dBm	2633 mV
-5dBm	3017 mV
0dBm	3421 mV

	(4.6) at ____ GHz
(4.2) TSS	41.0 dBm
TSS at 5MHz B.W. (4.3)	43.2 dBm

TSS should be better than -41.5dBm at 5MHz B.W.

TEMPERATURE PERFORMANCE

MODEL # LDX1002

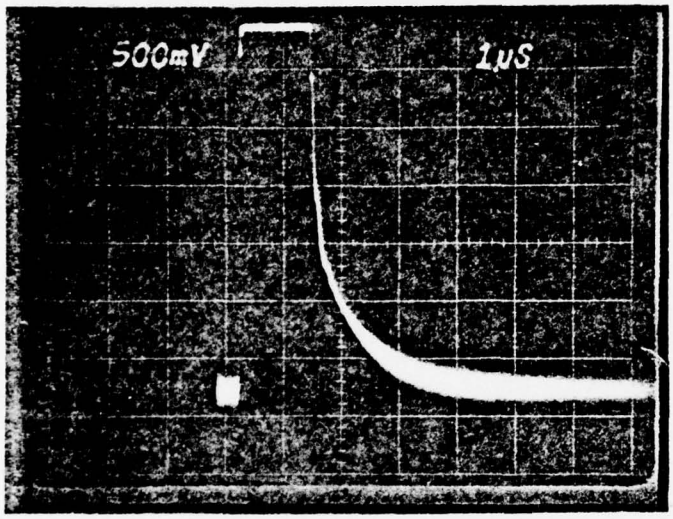
SERIAL # 16358

LOG LINEARITY

	OP AT +25°C	OP AT -54°C	OP AT +85°C
-40dBm	253 mV	233 mV	270 mV
-35dBm	600 mV	580 mV	633 mV
-30dBm	982 mV	926 mV	1006 mV
-25dBm	1406 mV	1360 mV	1420 mV
-20dBm	1830 mV	1721 mV	1815 mV
-15dBm	2237 mV	2096 mV	2231 mV
-10dBm	2633 mV	2505 mV	2628 mV
-5dBm	3017 mV	2902 mV	2997 mV
0dBm	3421 mV	3308 mV	3410 mV

MODEL # LDX1002

SERIAL # 16358



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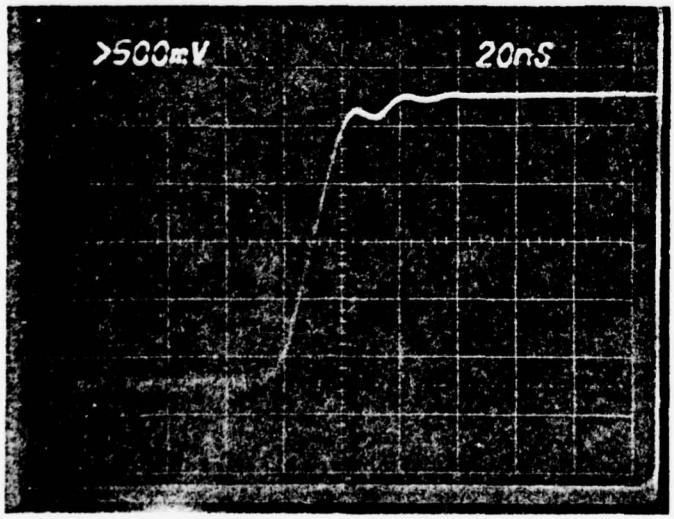

RISE TIME
AT 0 dBM INPUT

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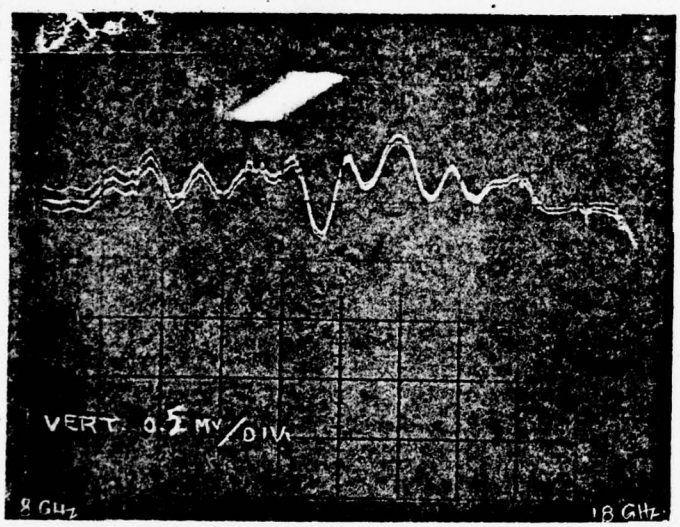
SERIAL # 16359-60



MODEL LDX1003
DETECTORS USED
SELECTED FROM
THE FOUR MATCHED
DETECTORS SHOWN
IN THE SWEPT RESPONSE
PHOTOGRAPH

MODEL # LDX1003

SERIAL # 16359

TEST RESULTS

(3.8)	DELAY TIME	25 nS (80nS max.)
(3.9)	RISE TIME	25 nS (80nS max.)
(3.10)	SETTLING TIME	60 nS (80nS max.)
(3.11)	PROPOGATION DELAY + SETTLING TIME	85 nS (140nS max.)

LOG LINEARITY

	(4.6) OP AT 10 GHz
-40dBm	306 mV
-35dBm	707 mV
-30dBm	1114 mV
-25dBm	1528 mV
-20dBm	1406 mV
-15dBm	2240 mV
-10dBm	2660 mV
-5dBm	3073 mV
0dBm	3389 mV

	(4.6) at ____ GHz
(4.2) TSS	39.5 dBm
TSS at 5MHz B.W. (4.3)	41.7 dBm

TSS should be better than -41.5dBm at 5MHz B.W.

TEMPERATURE PERFORMANCE

MODEL # LDX1003

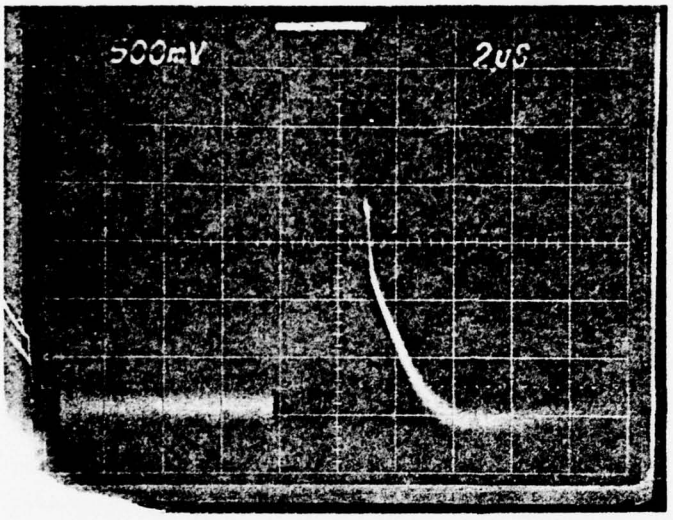
SERIAL # I6359

LOG LINEARITY

	OP AT +25°C	OP AT -54°C	OP AT +85°C
-40dBm	306 mV	428 mV	468 mV
-35dBm	707 mV	815 mV	811 mV
-30dBm	1119 mV	1190 mV	1160 mV
-25dBm	1528 mV	1585 mV	1546 mV
-20dBm	1906 mV	1964 mV	1420 mV
-15dBm	2240 mV	2285 mV	2281 mV
-10dBm	2660 mV	2709 mV	2707 mV
-5dBm	3073 mV	3135 mV	3110 mV
0dBm	3384 mV	3415 mV	3447 mV

MODEL # LDX1003

SERIAL # 16359



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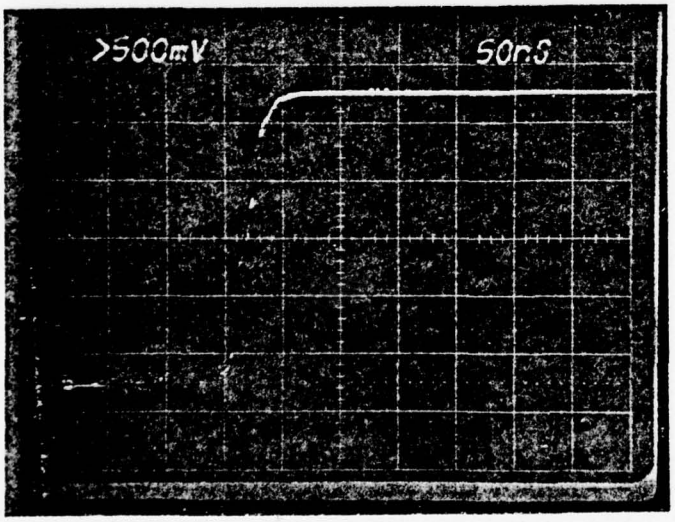
AT 0 dBM INPUT



RISE TIME
AT 0 dBM INPUT

MODEL # LDX1103

SERIAL # 16360

TEST RESULTS

(3.8) DELAY TIME	20 nS (80nS max.)
(3.9) RISE TIME	22 nS (80nS max.)
(3.10) SETTLING TIME	70 nS (80nS max.)
(3.11) PROPOGATION DELAY + SETTLING TIME	90 nS (140nS max.)

LOG LINEARITY

	(4.6) OP AT 10 GHz
-40dBm	368 mV
-35dBm	391 mV
-30dBm	1052 mV
-25dBm	1464 mV
-20dBm	1821 mV
-15dBm	2188 mV
-10dBm	2616 mV
-5dBm	3070 mV
0dBm	3367 mV

	(4.6) at 10 GHz
(4.2) TSS	39.5 dBm
TSS at 5MHz B.W. (4.3)	41.7 dBm

TSS should be better than -41.5dBm at 5MHz B.W.

TEMPERATURE PERFORMANCE

MODEL # LDX1003

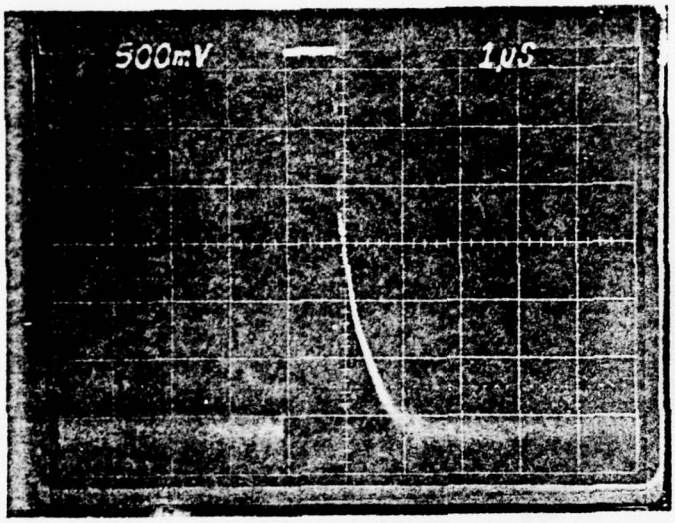
SERIAL # 16360

LOG LINEARITY

	OP AT +25°C	OP AT -54°C	OP AT +85°C
-40dBm	368 mV	243 mV	410 mV
-35dBm	691 mV	688 mV	744 mV
-30dBm	1052 mV	1117 mV	1065 mV
-25dBm	1464 mV	1538 mV	1453 mV
-20dBm	1821 mV	1901 mV	1850 mV
-15dBm	2188 mV	2251 mV	2218 mV
-10dBm	2616 mV	2691 mV	2637 mV
-5dBm	3070 mV	3181 mV	3080 mV
0dBm	3367 mV	3439 mV	3398 mV

MODEL # LDX1003

SERIAL # 16360



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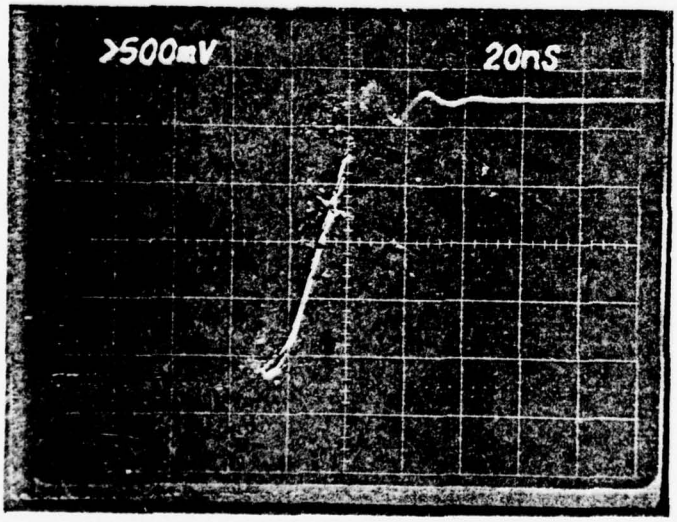

RISE TIME
AT 0 dBM INPUT

3.0 COMMENTS ON ACTUAL HARDWARE PERFORMANCE VERSUS PROJECT PERFORMANCES

Aertech Industries takes pleasure in reporting all the requirements of the program from an electrical performance standpoint were met, and in most cases, exceeded. Few parameters, which are significantly better than projected earlier are:

1) Rise time down to 20 nanoseconds as compared to a specification of 70 nanoseconds.

2) Recovery time at 0 dBm of less than 1.0 μ seconds, where as this parameter was not specified earlier. It is fair to point out that typical value of recovery time at 0 dBm runs anywhere from 10 to 20 microseconds.

3) Temperature performance, was well within specification, and extremely stable baseline.

4) Differential matching well within specification.

4.0 QUARTERLY PROGRESS REPORT

This covers the period ending November 30, 1973, as follows.

QUARTERLY PROGRESS REPORT

(period ending Nov. 30, 1973)

prepared for

U.S. Naval Research Laboratory
Washington, D.C. 20375

Contract No. N00014-74-C-0020
Req'n No. 00173-3-006371/2-27-73

prepared by

Aertech Industries
825 Stewart Drive
Sunnyvale, California 94086

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a. Program Planning
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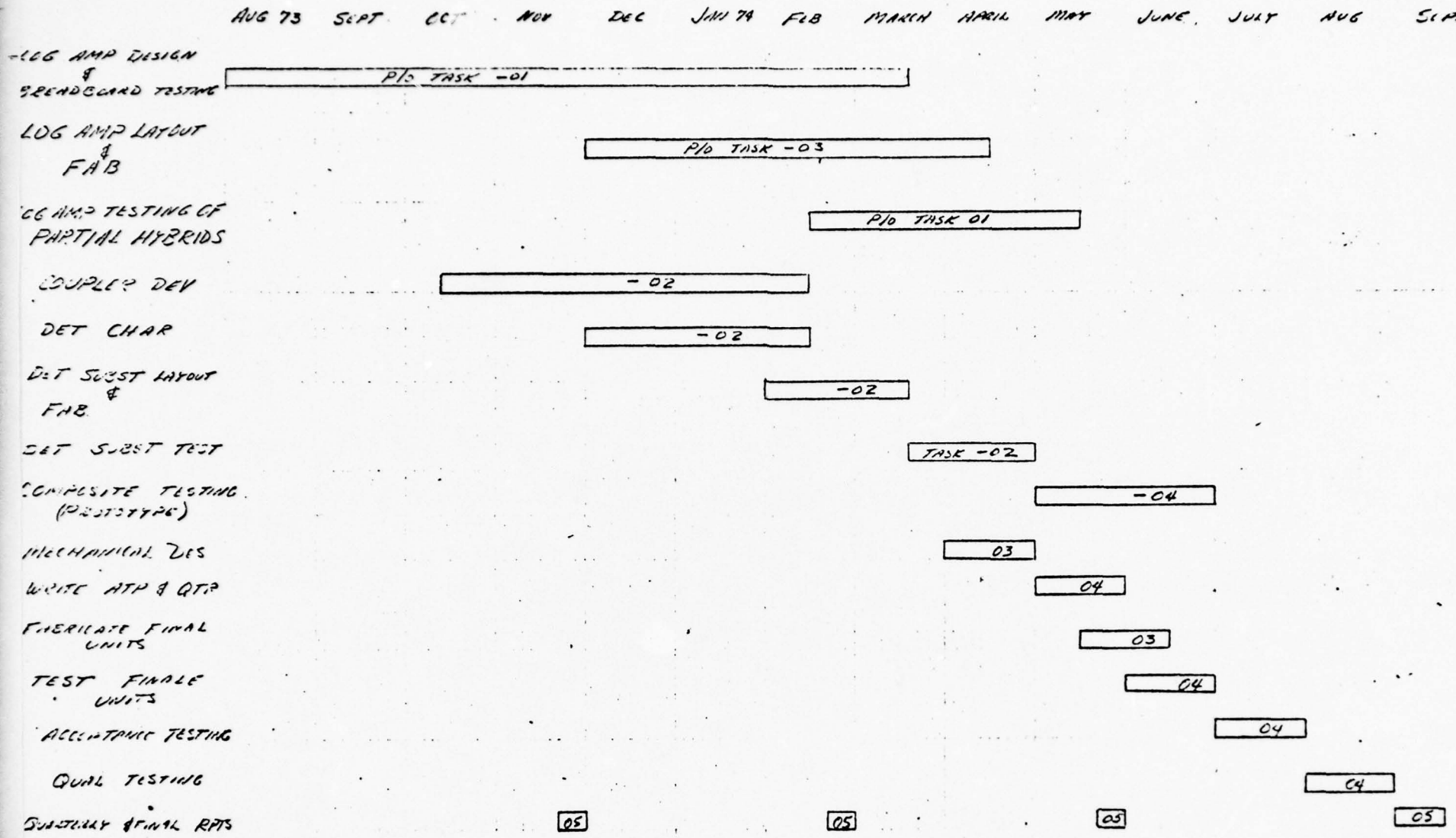

AUG 73
SEPT
OCT
NOV
DEC
JAN 74
FEB
MARCH
APRIL
MAY
JUNE
JULY
AUG
SEPT
LOG AMP DESIGN & BREADBOARD TESTING
P/O TASK -01
LOG AMP LAYOUT & FAB
P/O TASK -03
LOG AMP TESTING OF PARTIAL HYBRIDS
P/O TASK 01
COUPLER DEV
-02
DET CHAR
-02
DET SUBST LAYOUT & FAB
-02
DET SUBST TEST
TASK -02
COMPOSITE TESTING (PROTOTYPE)
-04
MECHANICAL DES
03
WRITE ATP & QTP
04
FABRICATE FINAL UNITS
03
TEST FINALE UNITS
04
ACCEPTANCE TESTING
04
QUAL TESTING
04
SUBSTUDY & FINAL RPTS
05
05
05
05

INTRODUCTION

This reporting period progress in the areas of 3dB couplers, microwave detectors, and amplifiers hybridization is discussed. Additionally, some discussion is directed to material and processing techniques in the area of thin film technology. The philosophy that is presently being followed is to develop and prove each component individually before mating it to its complement.

In the area of 3dB couplers a slight deviation from the proposal has been taken for the lower frequency band. The first iteration of this coupler has been an interdigitated version rather than two cascaded 8.34dB couplers as proposed. This type of coupler will be investigated first to determine if it is useable for this application. The higher frequency band coupler is of the interdigitated type as proposed. The technical section covers the performance obtained from the first iteration of these two couplers.

In the detector area individual circuits are discussed for the characterization of the Schottky detector diode. Since detector RF testing is going on at the present time there is no data included for detectors.

In the area of amplifier hybridization, discussion is directed to the power supply and three logging stages of the amplifier that have been laid out for thick film fabrication. The tradeoffs between thick and thin film fabrication as it applies to the circuit are addressed.

AMPLIFIER HYBRIDIZATION

The first layout of the power supply and three logging stages of the amplifier circuit has been completed. This circuit has three chip transistor arrays and two chip voltage regulators and two chip transistors. The circuit was laid out for thick film techniques using screend conductors and resistors with attached chip capacitors. This first iteration of the circuit is larger than anticipated and can be put on a ceramic substrate measuring 0.5 x 1.15 x 0.025 inches. The conductor and resistor inks are made by Electro Materials Corporation of America and are fired at the same temperature. Three resistor inks having a resistivity of 10, 300, and 3K ohms per square will be used to cover the wide range of resistor valves. The chip capacitors have a length and width of 0.050 inches.

Thick film techniques were picked over thin film techniques for this circuit because of the flexibility of the resistor aspect ratios. The resistors in this circuit range from 20 to 17K ohms. Since in thin film metalized substrates you can only get one value of resistivity in the resistive layer it is not practical to cover all the resistor values. The use of chip resistor and thin film circuitry would be a solution except that finding exact values may be difficult. Therefore, the logical choice was the use of thick film, where varied resistor inks are available and trimming the resistor to required value is not difficult. Table II summarizes the advantages and disadvantages of thick and thin film system as they apply to this circuit.

The thick film gold conductor pattern is 0.010 inches wide and the type of gold chosen has good wire bonding properties and solderability This width of conductor was chosen since line width are not critical and This size is easy to screen. Resistor values of 20 ohms to 36.5 ohms will be made with 10 ohms per square ink, resistor values of 200 ohms to 2K ohms will be made with 300 ohms per square ink, and resistor values

above 300 ohms will use 3K ohms per square ink. The resistors are designed to lower values of resistance so that they may be trimmed upwards in value. Interconnection between transistor chips and printed conductor will be done by wire bonding. Additionally, the use of wire bonds will be made to facilitate conductor paths where necessary.

A second iteration of this circuit is underway with the objective of reducing the size of the substrate. A new approach for laying this circuit out is the use of more chip arrays to simplify the conductor paths. This would simplify the topology problem and may reduce the substrate size a considerable amount.

For the next reporting period the circuit will be re-laid out using additional transistor array chips. Marks will be made for conductor and resistors and several circuits will be screened and fired and electrically tested.

Table II

Thick Film Versus Thin Film Technology		
SYSTEM	ADVANTAGES	DISADVANTAGES
Thick Film	Resistor aspect ratio flexibility resulting in small size substrate.	Poor line resolution.
	All resistor values can be met using different inks.	One mask required for each ink used.
Thin Film	Good line resolution.	Poor resistor aspect ratio flexibility resulting in larger substrate sizes.
	Maximum of two masks required.	Require use of chip resistor to meet all resistor values.

COUPLERS

The first iteration of two interdigitated type microstrip coupler design have been fabricated and RF tested. These circuits were fabricated on metalized alumina substrates having dimensions of 0.5 x 0.5 x .025 inches using thin film techniques. Figure 1 shows the configuration of the interdigitated couplers. The couplers are designed to cover the frequency ranges of 2.6 to 8 GHz (S/C Band) and 6.9 to 18 GHz C/Ku which corresponds to a fractional bandwidth of 102% and 89.5% respectively.

The circuits were etched on 99.5% pure alumina substrates which were metalized by sputtering with 150 angstroms of chromium and 300 microinches of gold. The substrates had a surface finish of four microinches CLA and the finger of the couplers were stitched with 0.7 mil diameter gold wire. The average line width and gap width dimension are listed in Table 1. The coupler configuration and dimensions were arrived at by scaling from existing operational designs. The designs are based on empirical work that previously yielded working circuits.

Table 1

Band	Frequency (GHz)	Line Width w (mils)	Gap Width "g" (mils)
1	2.6-8.0	3.7	1.8
2	6.9-18.0	3.5	1.18

The circuits were etched and wire stitched using a wedge bonder in the diode etching and assembly area of Aertech. Some difficulties were encountered in the stitching of the couplers that results in longer than anticipated wire loops and damage to the lines. This was attributed to operator inexperience in bonding this type of structure.

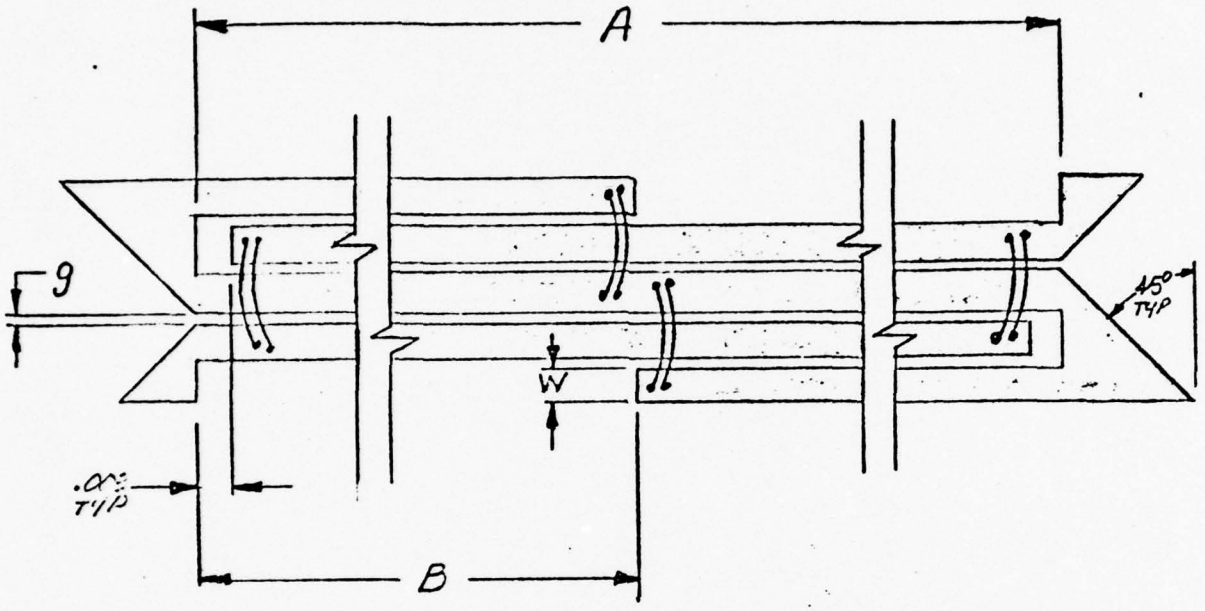


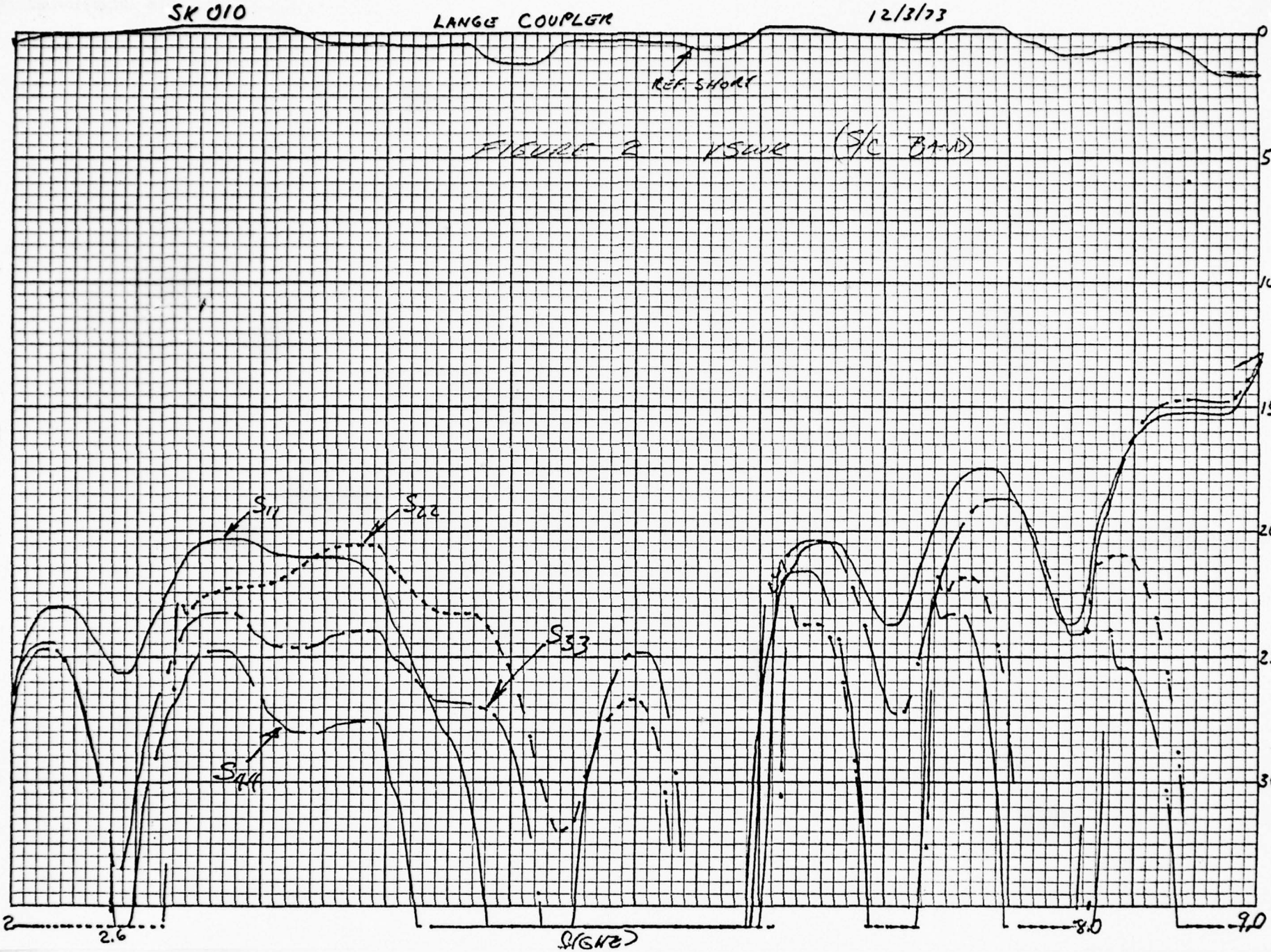
FIGURE 1

3dB COUPLER

The RF performance obtained by the S/C Band unit is shown in Figure 2,3,and4. The data shows a maximum VSWR of 1.33 to 1 and a minimum isolation of 20dB. The coupling is approximately 3.3dB except for the lower end of the band where the coupling is much worse than expected in the order of 5dB for the coupled port. The coupling can be improved by adjusting the line and gaps to give tighter coupling and improving the wire stitching.

The C/Ku band unit performance is shown in Figures 5,6,7,8 and 9. The worst VSWR occured at 14GHz and was 2.6:1. This is directly attributed to the poor stitching of the coupler. The isolation was 13dB worse case and the coupling averaged about 4dB, the coupled port was 5.4dB at the lowest frequency. This circuit can also be improved by adjusting the line and gap width and improving the stitching. The performance was worse on this circuit because its high frequency operation makes stitching and dimensional tolerance more critical.

For the next quarter, the second iteration of these circuits will be fabricated and tested. The line and gap width will be adjusted to give tighter coupling. Additionally, the wire stitching will be improved to give better performance especially at the higher frequencies. The wire stitching will be improved with the purchase of a new thermocompression ball bonder.



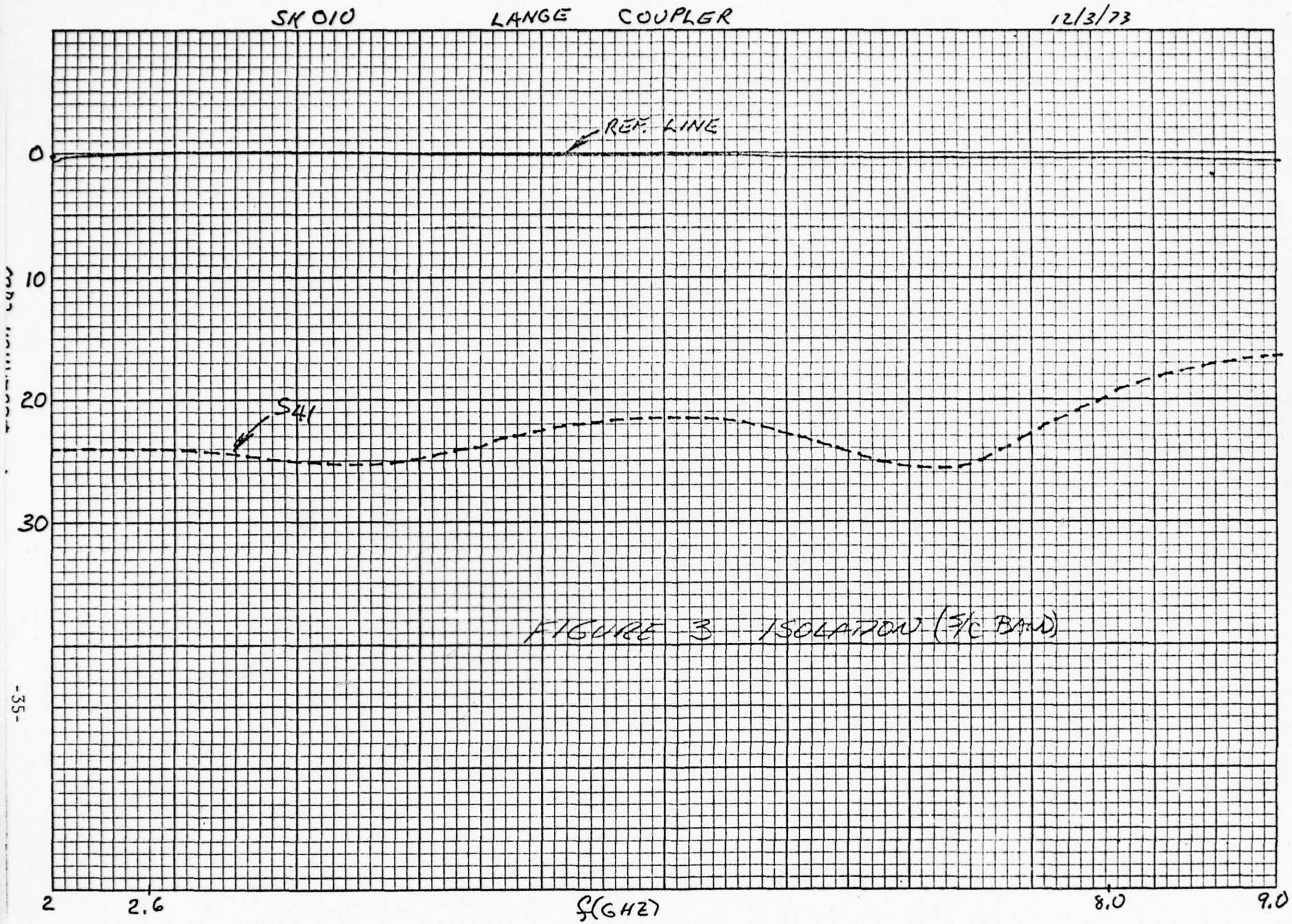
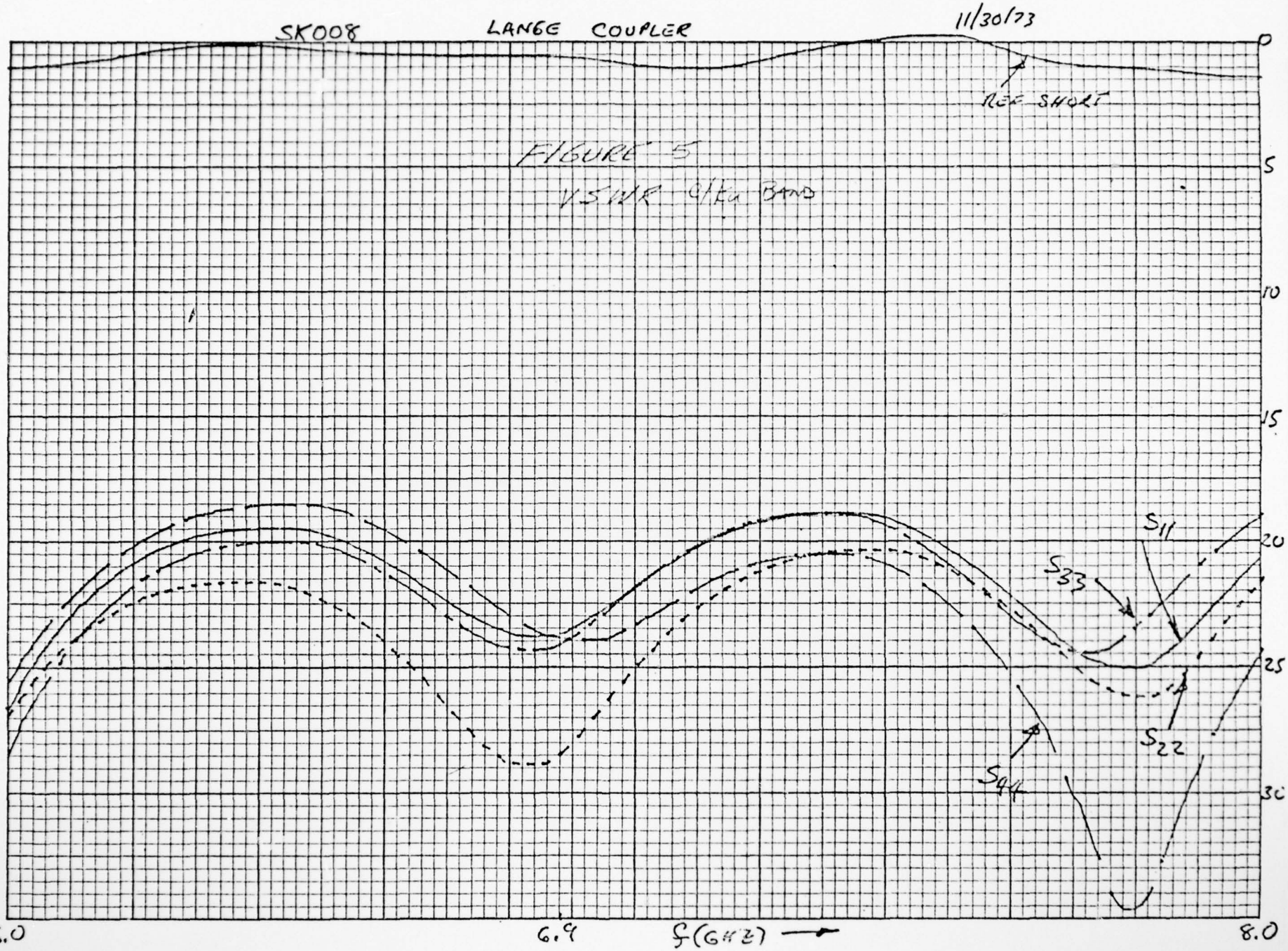


FIGURE 3 ISOLATION (F/C BAND)



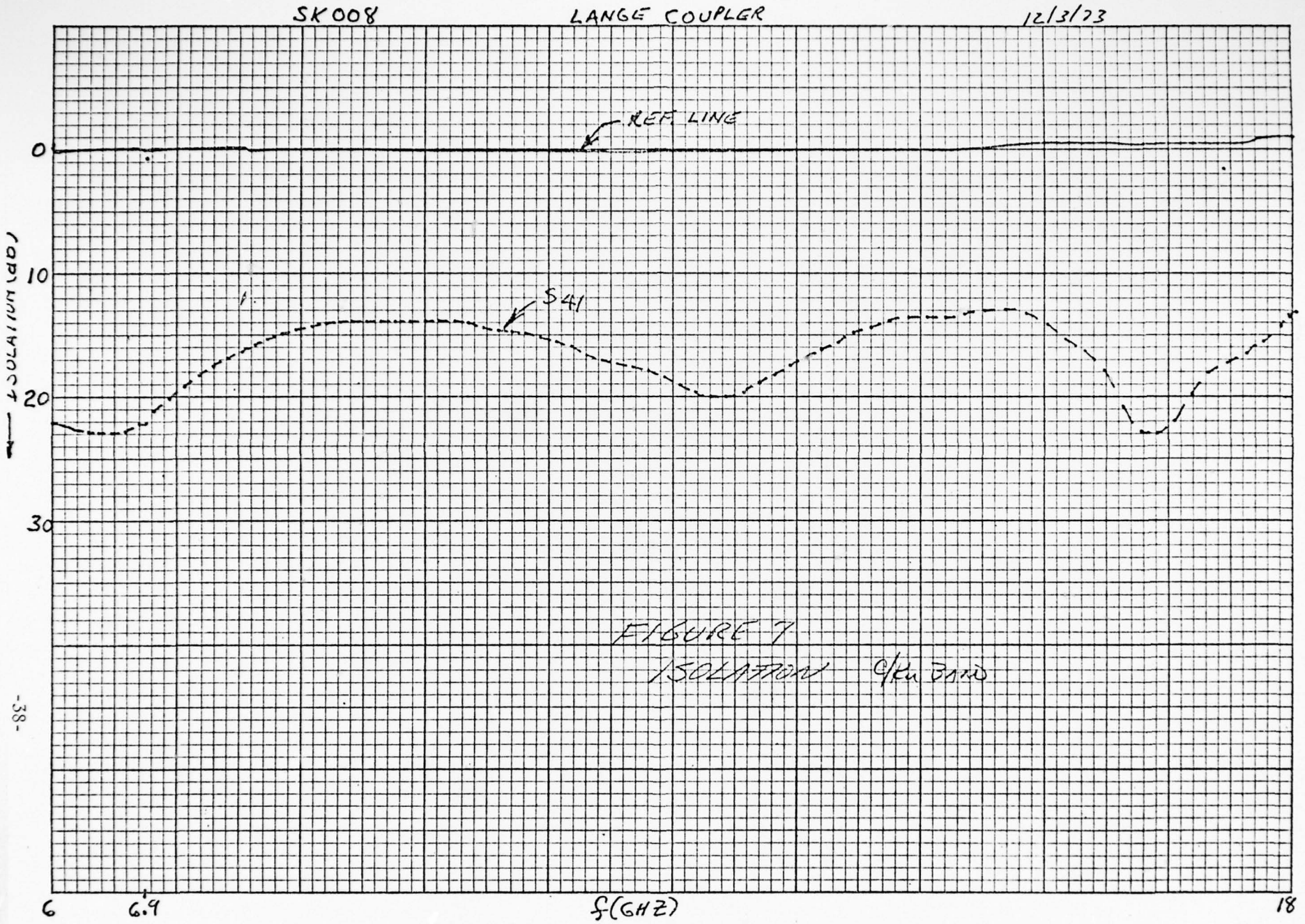
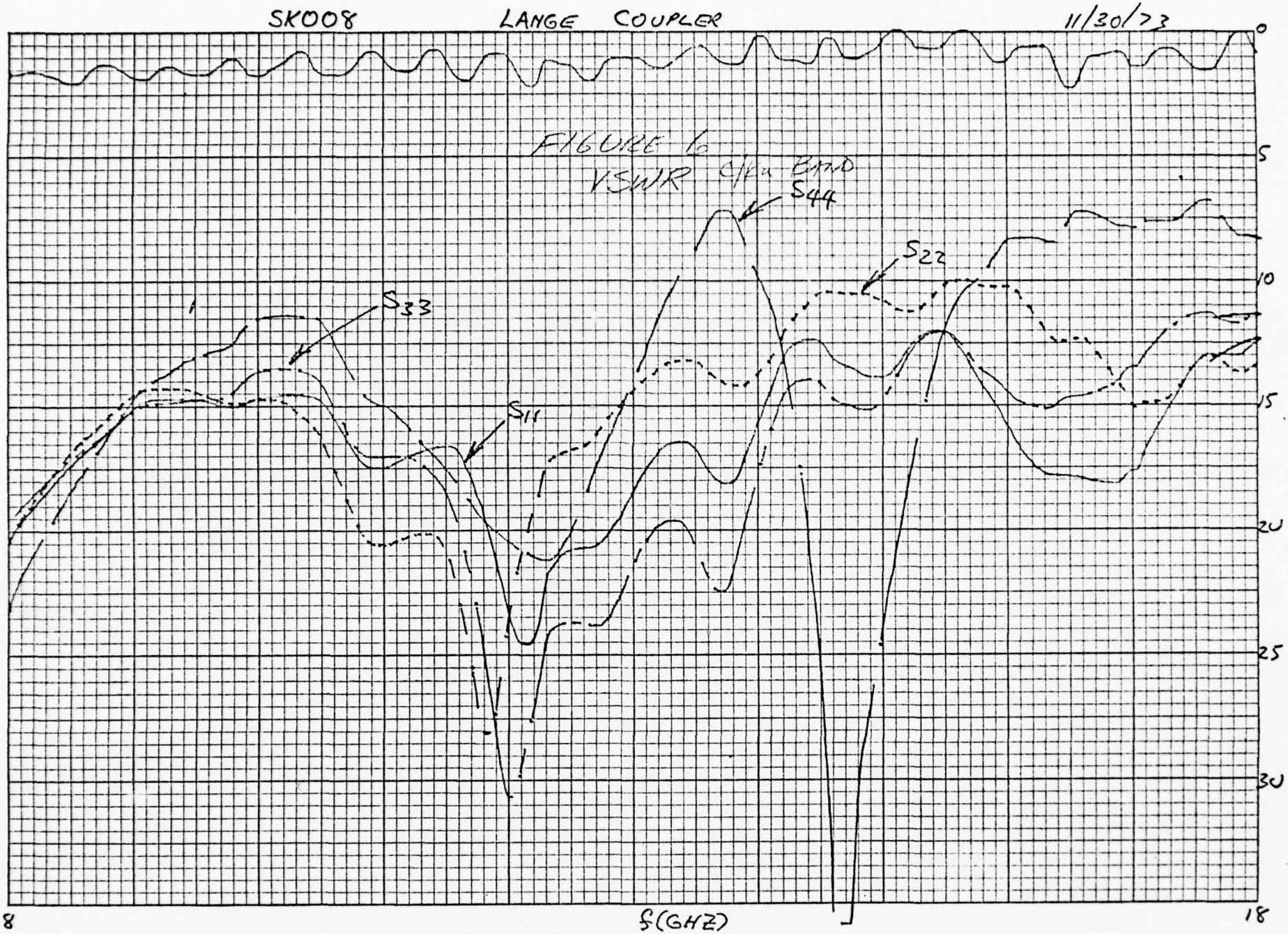
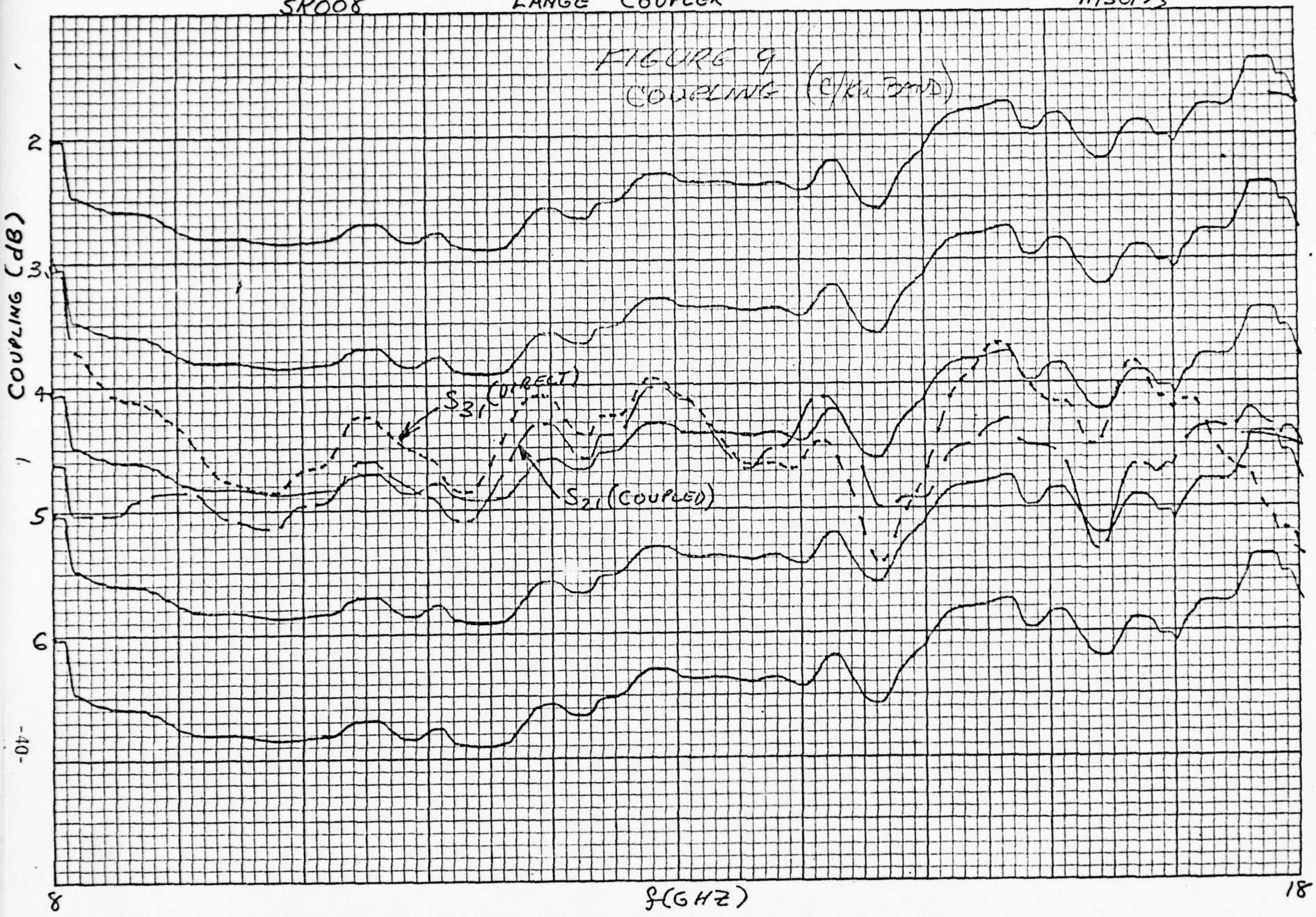


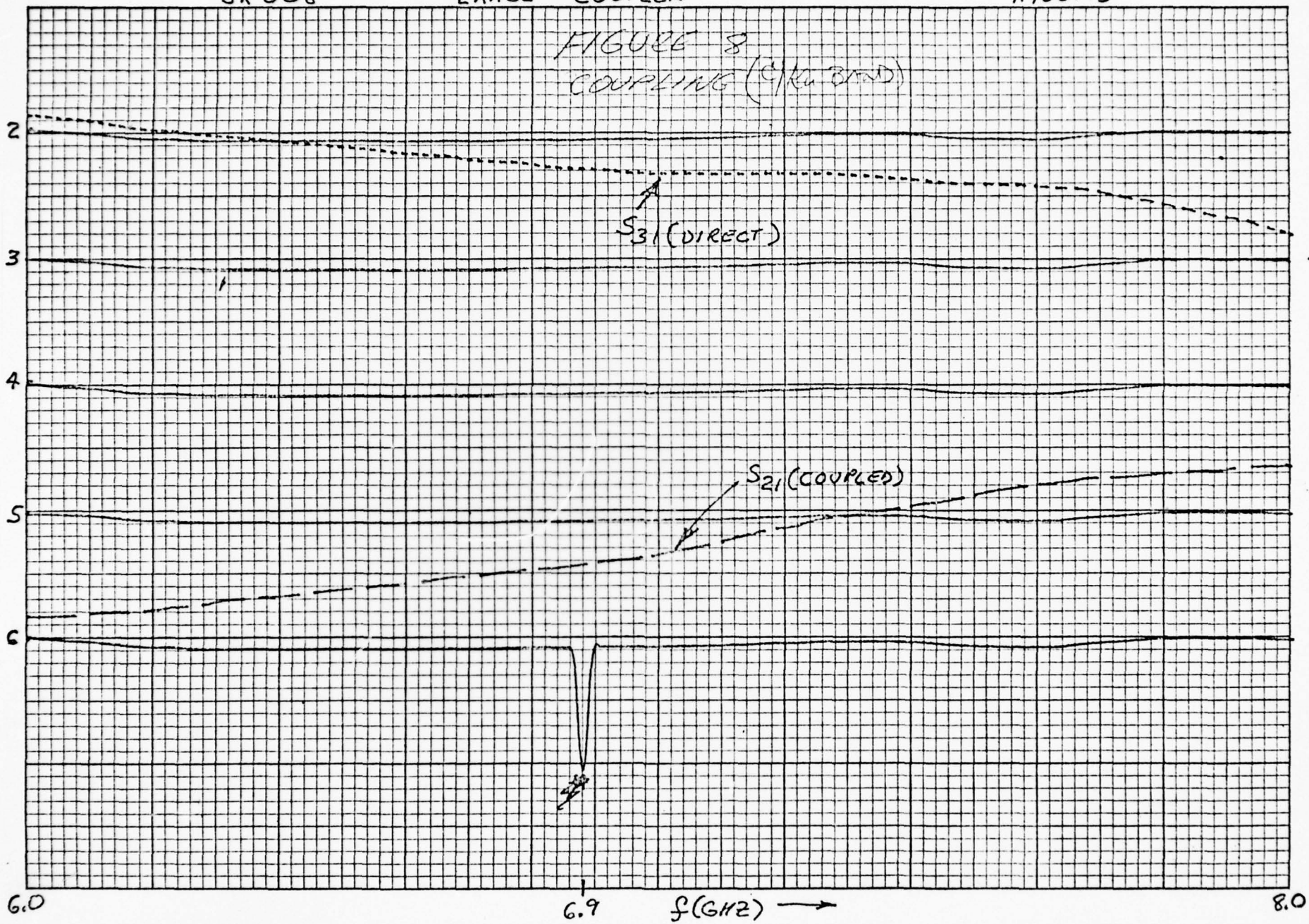
FIGURE 7
ISOLATION C/Ku BAND



SK008 LANGE COUPLER 11/30/73



SK008 LANGE COUPLER 11/30/73



DETECTORS

Detector characterization circuits have been designed and etched during this reporting period. The diode characterization circuits were fabricated on 99.6 pure alumina substrates metalized with chrome gold. The circuits consist of 50Ω input lines with an etched bypass capacitor in one circuit or another circuit where the diode is attached to ground directly. These circuits will be used to characterize the impedance and diode voltage sensitivity as a function of frequency of the detector diode that will be used on the detector circuit. Also, a companion circuit has been fabricated that is the exact replica of the diode to provide a short reference which is identical to the diode test fixture.

Additionally, detector circuits have been designed and the artwork made which uses an etched tantalum nitride resistor in front of the diode. These tests are now in progress but as yet there is no available data to present this reporting period.

Next reporting period the diodes shall be characterized and several configurations of detector circuit will be tested and reported on. Additionally, an evaluation of tantalum nitride resistor as a function of frequency and aspect ratio will be made.

Also, standard laboratory holders have been designed and fabricated to test the microwave prototype circuits. Having standard holders for each substrate size will reduce the variation in test results that could occur if different types of holders were used for each circuit. These circuit holders are machined out of brass and have the threaded type of microstrip end launchers. The end launchers are made by Cableway Systems and have a maximum VSWR of 1.20:1 to 18 GHz.

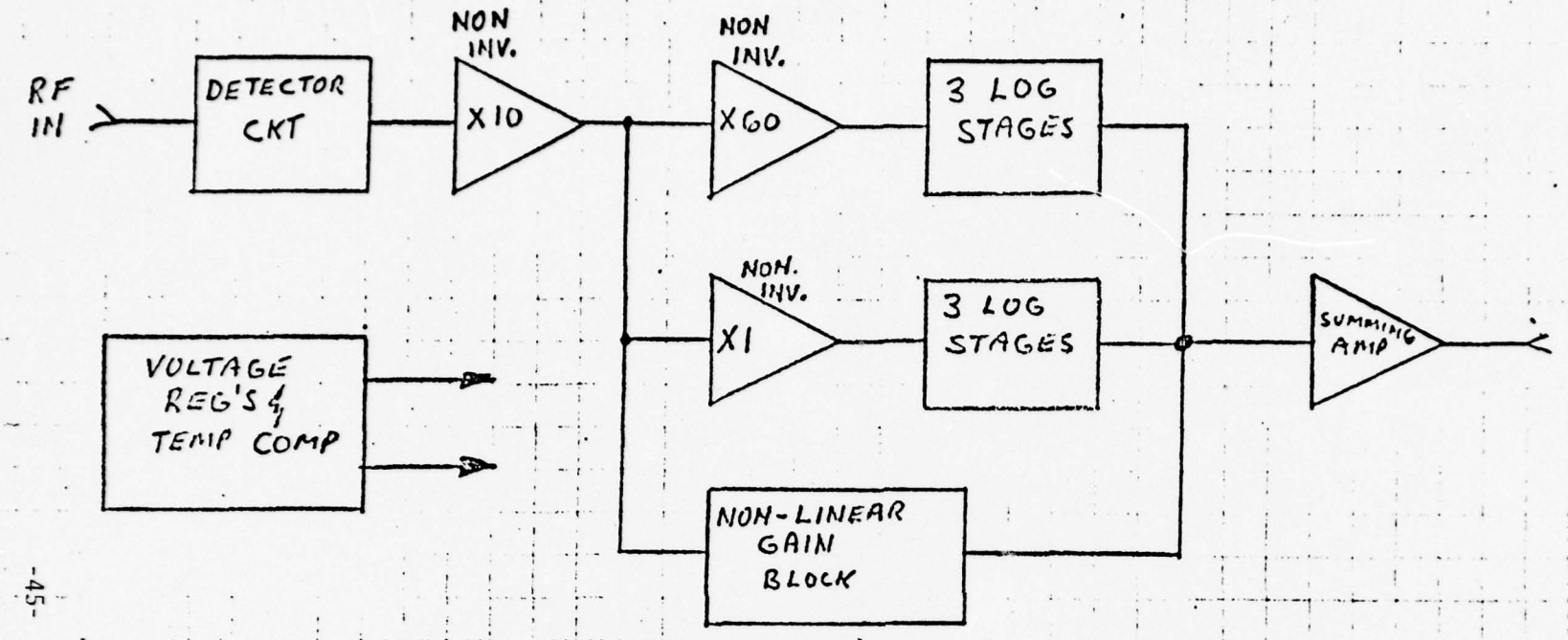
For the next reporting period it is anticipated that a 0.0002 to 0.00025 inches etch factor will be achieved by refinement of our etching techniques.

TECHNIQUES

During this reporting period considerable effort was expended with two suppliers of metalized substrates so that Aertech is assured of high quality alumina substrates. The substrate sizes that will be commonly in use are 0.5 x 0.5 x 0.025 inches, 0.5 x 1.0 x 0.025 inches, 1.0 x 1.0 x 0.025 inches and 1.0 x 1.50 x 0.025 inches, having a surface finish of 4 microinches centerline average (CLA). This surface finish provides the best compromise between metal adhesion properties and RF circuit performance up to 20 GHz. It is intended that chromium/gold, and tantalum nitride/chromium/gold, metalizations will be used for microwave circuit fabrication. The tantalum nitride layer will be used for etching resistors as they are required in the microwave circuit.

Photolithographic work is being handled by outside vendors presently. A maximum of three-day turnaround has been experienced thus far with 1/2 day turnaround time being requested and gotten on one occasion. Negative type of masks are currently being utilized for the microwave circuits.

Additionally, during this reporting period thin film substract ive procedures were established for exposure time, development time, and etching times for microwave circuits on metalized ceramic substrates. The techniques that were established apply to the negative type of photoresist manufactured by Kodak. The amount of variation between mask and etch circuit dimensions "etch factor" has been 0.0005 inches thus far. The target for etch factor is 0.0002 to 0.00025 inches and it is anticipated that we will achieve it shortly. Potassium Iodine type of solutions are being used for etching gold and Hydrochloric acid types are used for etching chromium. Tantalum nitride is being etched with a solution containing hydrofloric acid. All of the etchant solutions are mixed at Aertech.



BLOCK DIAGRAM

INTEGRATED DETECTOR--LOG VIDEO AMPLIFIER

FIGURE 2.

In Figure 3 it is assumed that power supplies V_{CC} and V_{EE} are constant over the operating temperature range.

It can be seen from the figure that if

$I_B = o$, then;

$$I = \frac{V_{Q_{3E}} + V_{EE}}{R_3} \qquad \text{----------1}$$

$$V_{Q_{3E}} = V_{Q_{3B}} - 0.7$$

$$V_{Q_{3B}} = V_{Q_{4B}} = 0.7 + R_2 \left(\frac{V_{CC} + V_{EE} - V_{Q_{4BE}}}{R_1 + R_2} \right)$$

If Q_3, Q_4 are matched, then their base emitter voltages track over temperature. Thus over temperature, quantity $\frac{\partial I}{\partial T}$ is very small

NUMERICAL ILLUSTRATION

$$V_{CC} = V_{EE} = 6.0V$$

$$R_2 = 3K,\ R_1 = 8.3K,\ R_3 = 750$$

then $I_1 = \frac{6 + 6 - 0.7}{8.3 + 3.0} = 1.0$ mA

$$V_{Q_{3B}} = 2.3 \text{ volts}; \quad V_{Q_{3E}} = -3.0V$$

or $I = \frac{3000}{750} = 4.0$mA

If operating temperature is -55°C and $\frac{\partial V_{B_E}}{\partial T}$ = -2mv/°C ΔT from 25°C = 80°C

then

$$I_1 \text{ @ } -55°C = \frac{6 + 6 - 0.86}{8.3 + 3.0} = 0.98 \text{ mA}$$

or $V_{Q3E} = V_{Q4E} = 3.042$

or $I = \frac{2957}{750} = 3.94$ mA

% change in I from 25°C to -55°C = 1.4%

It should be pointed out that in figure 3 R_1 , Q_4 , R_2 chain is used to bias only one transistor and the assumption $I_B = O$ is quite valid. However, when about 20 transistors are biased using the above chain then resultant cumilative change in the above bias current severly changes V_{Q_E} where Q is any one transistor out of a set of 20. This change results in a significant $\frac{\partial I}{\partial T}$ where I is the current provided by the constant current source in each differential pair. A biasing circuit was designed to drive up to 30 transistor current sources with insignificant $\frac{\partial I}{\partial T}$. Circuit is shown in the figure 4.

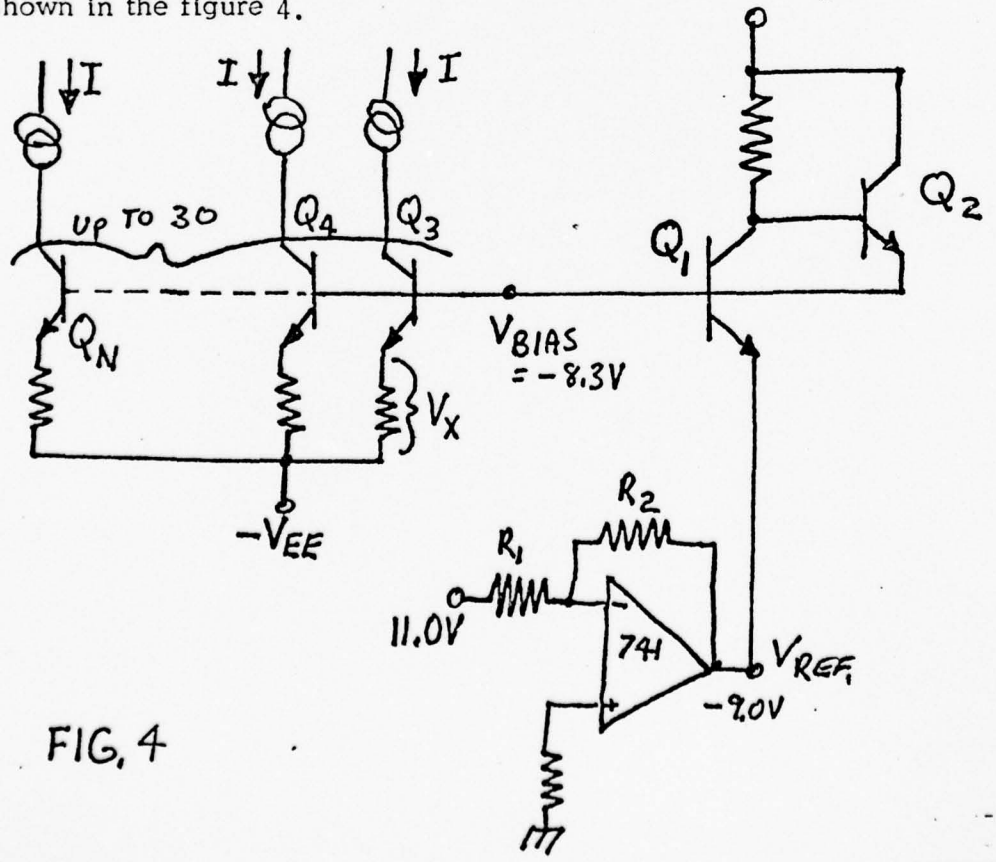


FIG. 4

An opamp (741) is used in the inverting mode to get a low impedance (A C. and D.C.) stable reference voltage $V_{Ref.}$ Q_1, Q_2, Q_3 --- Q_N are all matched transistors, thus their V_{BE}'s track over temperature within ±0.5 mV. Transistor Q_2 is used to supply the base current of transistors Q_3, Q_4, ---- Q_N.

Thus over temperature voltage at $V_{Q_{3E}}$, $V_{Q_{4E}}$----$V_{Q_{NE}}$ is going to be as constant as $V_{Ref.}$ Experimentally the above circuit shows less than 0.1% variation in $V_{Q_{3E}}$ etc.

GENERALIZED GAIN CELL

The following circuit shows a generalized block for gain 50, wide band amplifier.

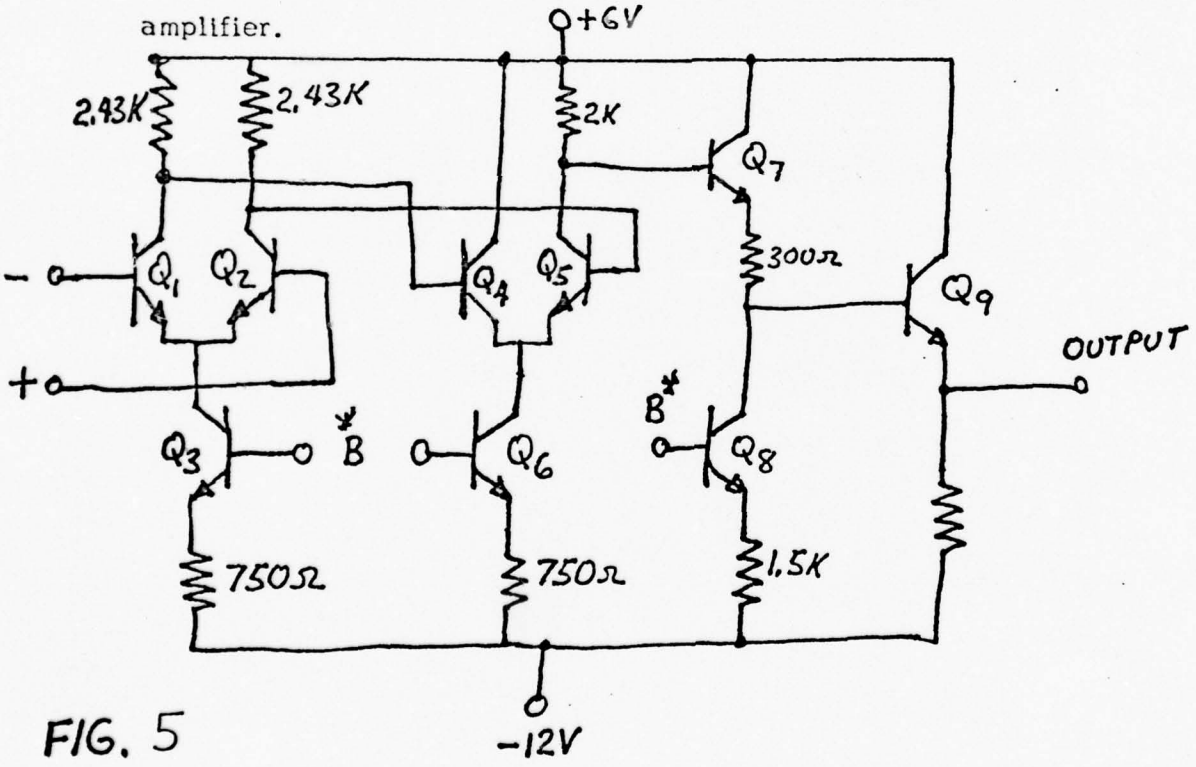


FIG. 5

*B represents bias voltage (derived from the circuit described earlier).

B = -8.3 Volts

From input output standpoint, the above circuit can be represented by:

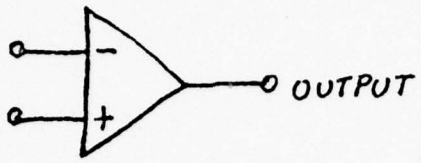


FIG. 6

It can be used in the inverting or the noninverting mode. A typical connection for X50 Non Inverting amplifier is:

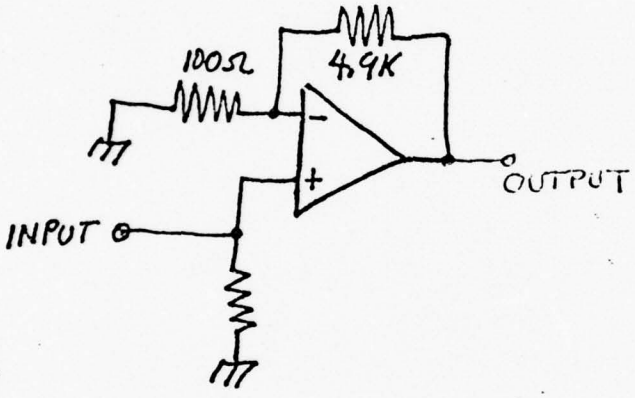


FIG. 7

Above circuit is designed to achieve wide bandwidth, linear and very low output offset drift. Each differential pair is biased at 2 mA/transistor to maximize the transistor f_t. Open loop voltage gain is:

$$\underset{\text{first diff. pair}}{(\text{gain})} \times \underset{\text{2nd pair}}{(\text{gain})}$$

First pair gain $\simeq \frac{2.43 \times 10^3}{26}$

Second pair gain, $\simeq \frac{2.0 \times 10^3}{26}$ =

Net open loop voltage gain $\simeq \frac{2.43 \times 2.0 \times 10^6}{26 \times 26}$

To keep offset drift very low, in addition to the high open loop gain, current through each differential pair and transistor Q_7 is kept very nearly constant over temperature by the biasing arrangement described earlier.

Results for the above circuit over temperature are described in a later section on the development of high gain linear amplifier.

Experiment to study the effect on the output log response of differential and common mode signals applied to the log stage.

The purpose of the experiment was to find out how a log stage with its associated summing amplifier would respond to common mode and differential signals. Theoretically speaking a common mode input voltage at the bases of a differential pair (without upsetting the biasing constraints) should not produce any change in the output.

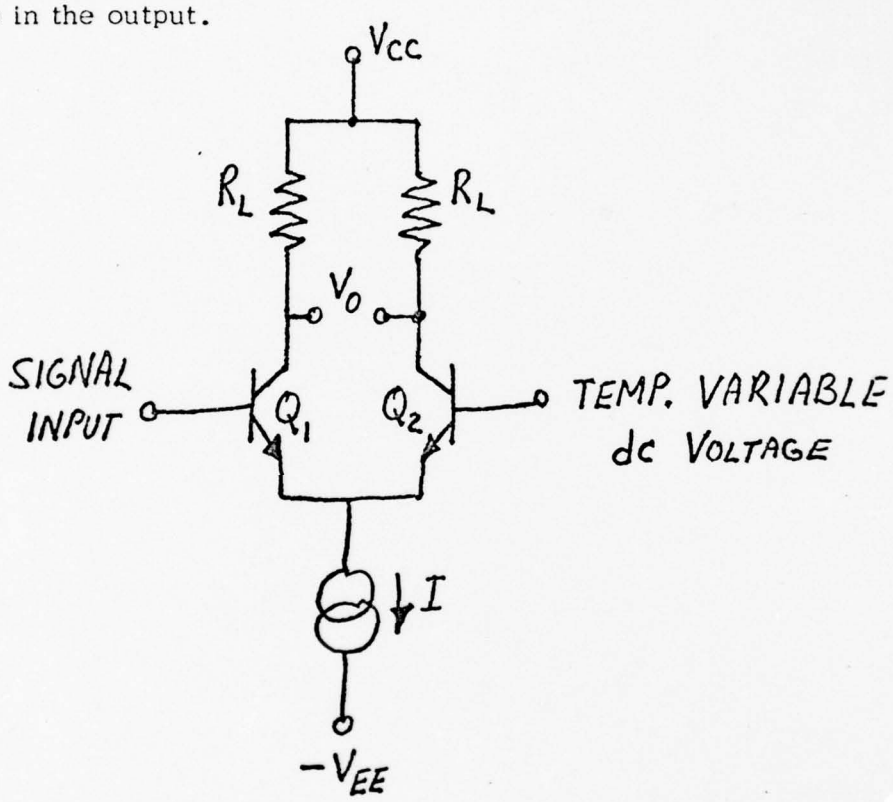


FIG. 8

Figure 6 shows a simple differential pair. Signal (A.C. signal + d.C. offset drift) is applied at the base of Q_1 . If the DC voltage at the base of Q_2 is made equal to the d.C. offset drift over temperature, then V_o shall remain constant over temperature and will be result of only the A.C. signal input. Essentially it

means injecting an external temperature variable d.C. voltage at $Q2_{base}$ so that the d.C. offset drift associated with the signal shall appear as common mode voltage to the differential pair and thus will be rejected. Test circuit for checking the common mode response is shown in figure 9.

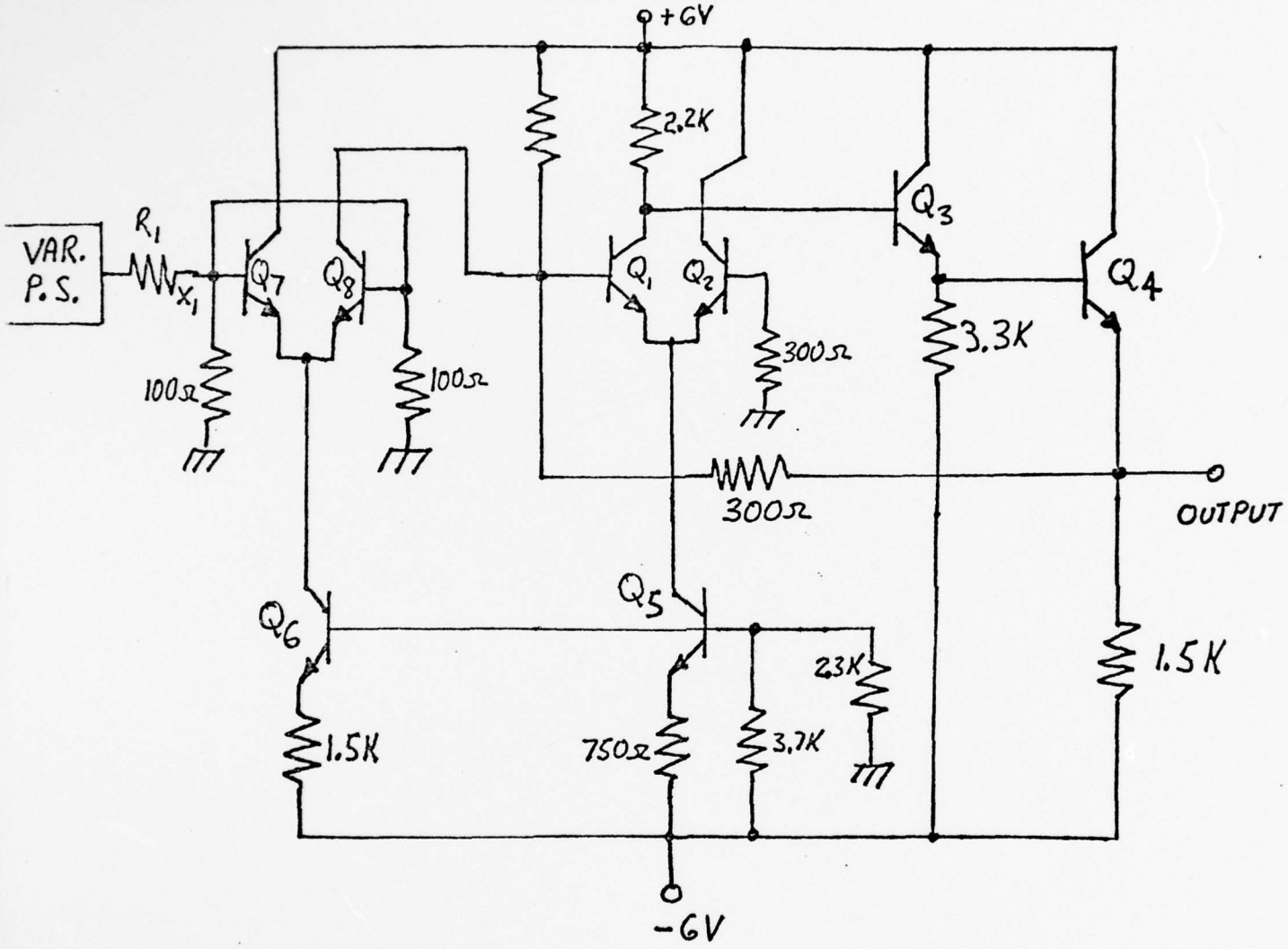


FIG. 9

Transistors Q_1, thru Q_5 form a fast summing amplifier. Q_7 - Q_8 form the logging stage. $R_1 \gtrsim 10K$

To apply common mode signal both bases are shorted together - Power supply voltage is varied to create the offset voltage at the point X_1.
Results are given below:

offset at point X_1	out put offset
+15.50 mv	-58.3 mv
+6.50 mv	-58.22 mv
-18.0 mv	-58.27 mv
- 6.0 mv	-58.24 mv

After the above successful test, the following test circuit was used to inject d.C. offset plus signal at the base of Q_7 and to apply the same d.C. offset at the Q_8 base from an independent source

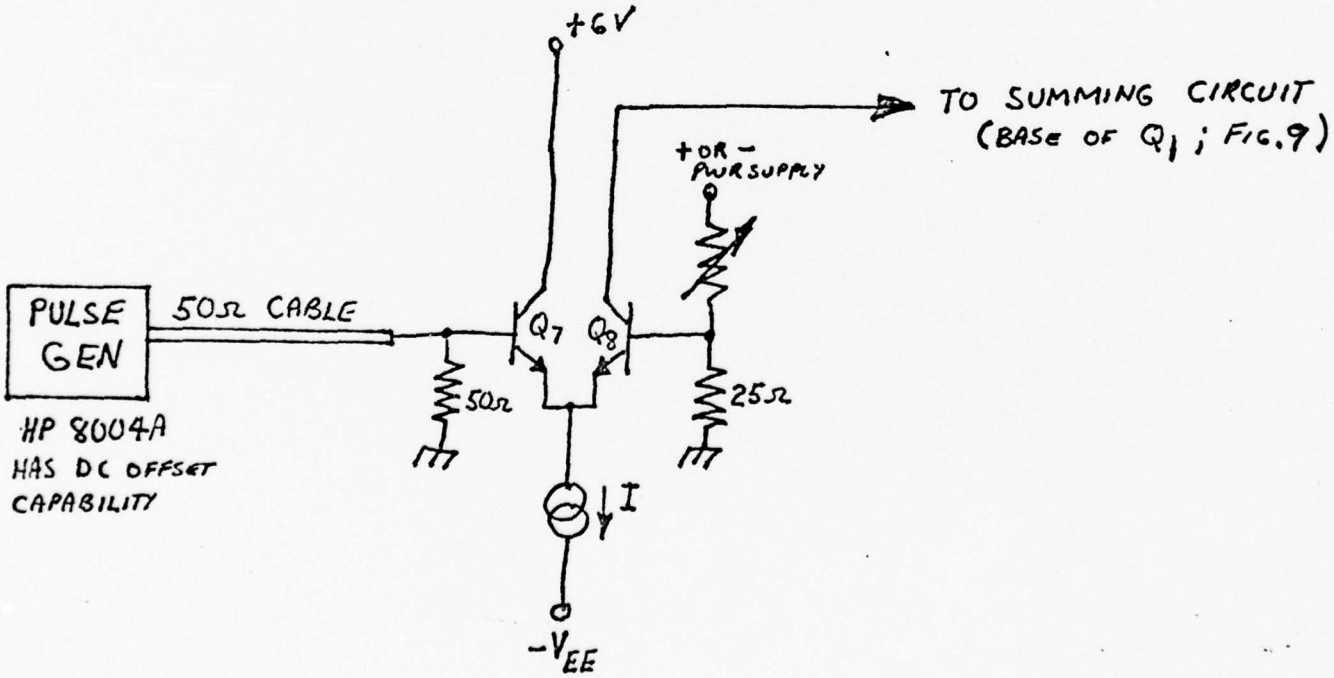


FIG. 10

Results were:

DC offset @		Input pulse (-ve) amplitude	Output Pulse amp	Output offset
$Q_{7_{base}}$	$Q_{8_{base}}$	$Q_{7_{base}}$		
6.0 mv	6.0 mv	10 mv	46 mv	-59 mv
"	"	20 mv	89 mv	"
"	"	50 mv	190 mv	"
"	"	100 mv	260 mv	"
+12 mv	+12 mv	10 mv	45.5	"
"	"	20 mv	89.0	"
"	"	50 mv	190.0	"
"	"	100 mv	255	"
-6 mv	-6 mv	10 mv	46	"
"	"	20 mv	90	"
"	"	50 mv	187	"
"	"	100 mv	255	"
-12 mv	-12 mv	10 mv	45.5	"
"	"	20 mv	90	"
"	"	50 mv	190	"
"	"	100 mv	255	"

Output pulse amplitude varies from 46 mv (Av.) to 260 mv (Av.) when input goes from 20 mv (-33.97 dBv) to 100 mv (-20 dBv), implying a log slope of 15.3 mv/dBv It is clear from the above data that first order cancellation of the dC offset drift effect on log output can be achieved by injecting an independent but temperature variable voltage on the $Q_{8_{base}}$.

Since in an actual circuit it is not possible to completely cancel the effect of dC offset drift, test circuit shown in figure 11was used to study the output log response with no correction voltage applied. This would in fact simulate the

the effect of the resultant differential drift between the two bases, when actual correction voltage is used.

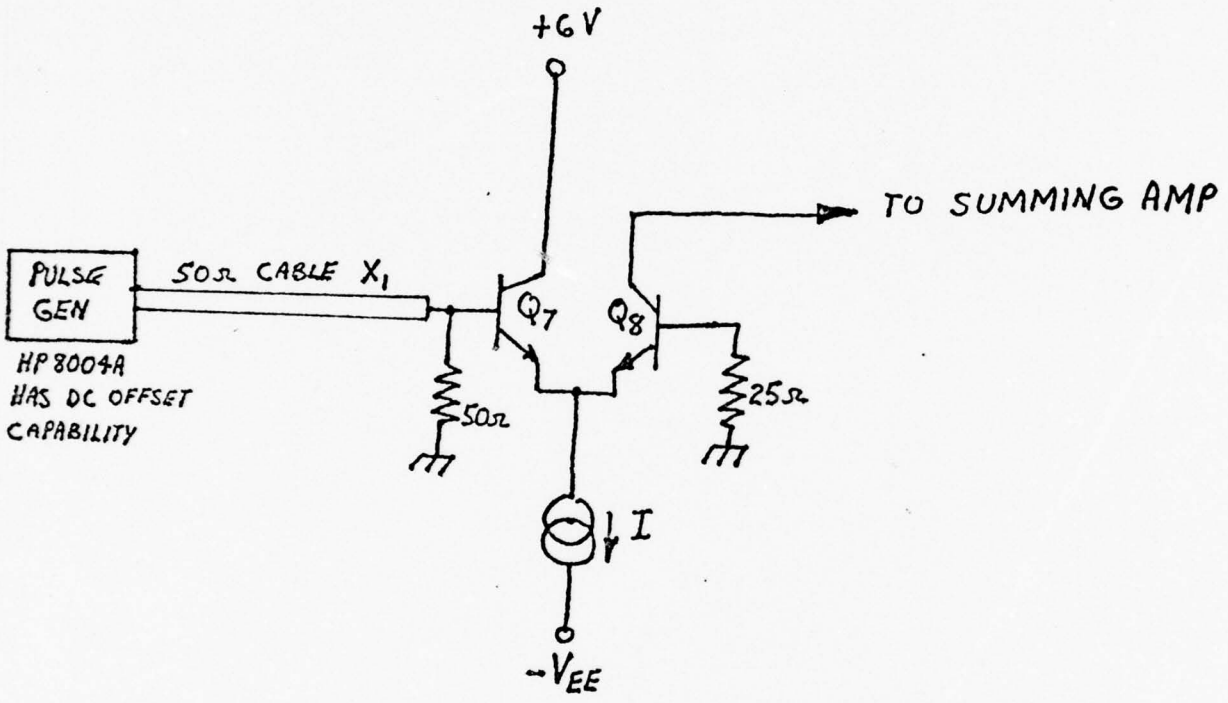


FIG. 11

Results achieved are tabulated below:

Input offset @$Q_{7_{base}}$	Input Pulse Amp @ $Q_{7_{base}}$	Output Pulse Amp.	Output Offset	Output Peak val e
0 mv	20 mv	104 mv	0	104 mv
	50 mv	230 mv	0	230 mv
	100 mv	333 mv	0	333 mv
-12 mv	20 mv	98 mv	+63 mv	161 mv
	50 mv	202 mv	"	265 mv
	100 mv	285 mv	"	348 mv
+12 mv	20 mv	106 mv	-63 mv	43 mv
	50 mv	249 mv	"	186 mv
	100 mv	375 mv	"	312 mv

Development of High Gain Linear Amplifier

As was pointed out in Aertech proposal (P-34238), high gain, low drift and wide band amplifier was one of the main blocks to be developed. Initially configured block diagram with a gain of 500 and meeting the above specified design objectives is shown below.

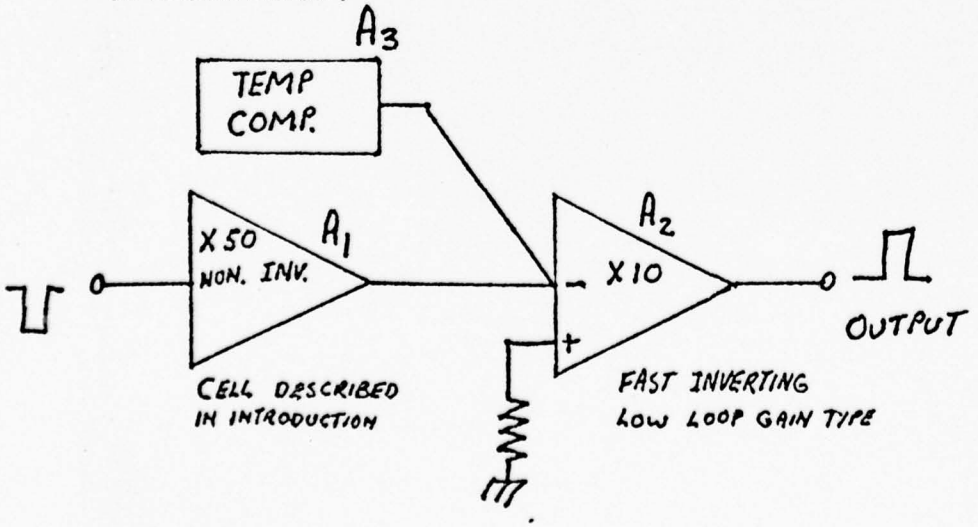


FIG. 12

It was expected that X50 amplifier being high loop gain type would give low but linear output drift. Typical rise time expected out of A_1 was 15 nonoseconds. To conserve bandwidth, A_2 was designed with moderate loop gain, and very fast bandwidth. From earlier work done at Aertech, it was known that A_2 type amplifiers have relatively large but very linear drift (up to 100 μv/°C refered to the input). Using the scaled down but very linear temperature variation of V_{BE} in a diode, it was expected to significantly null out the overall offset drift using the temperature compensation amplifier.

Detailed circuits for the above three blocks are described below:

A_1: Circuit and operation described in the introduction

A_2:

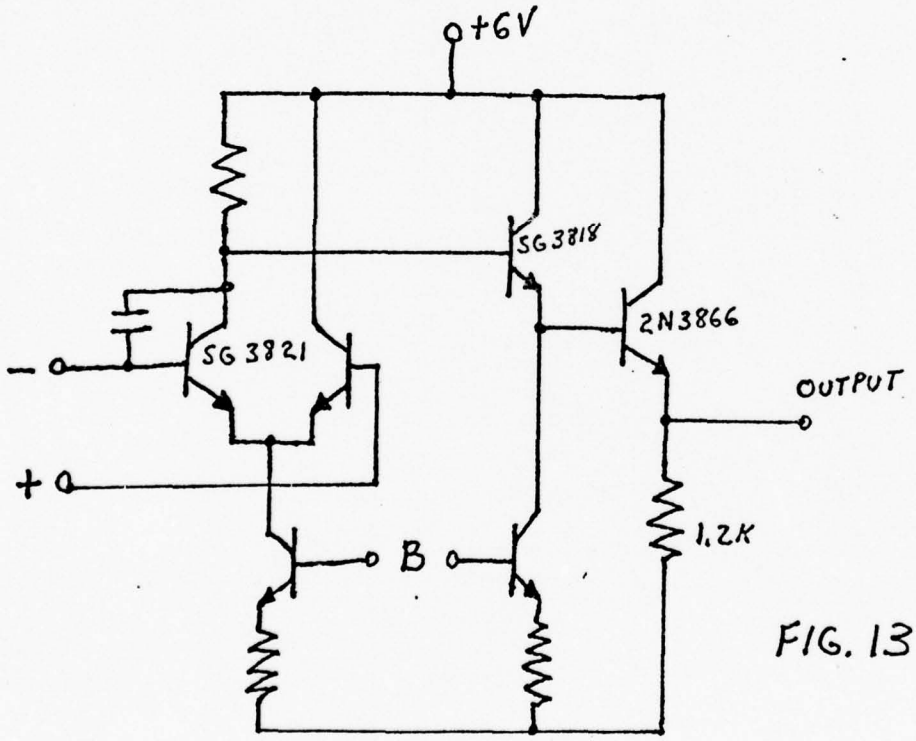


FIG. 13

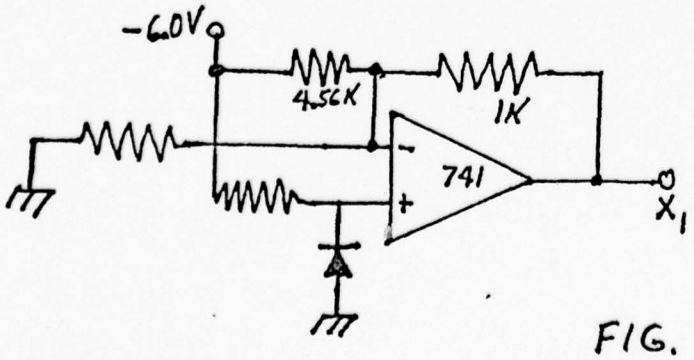


FIG. 14

In figure 14, X_1 is an output point with low dC. and A.C. impedance. At room temperature it is $\tilde{\tilde{=}}$ 0 ± 5 mv. Over temperature X_1 varies at $\tilde{=}$ 4.0 mv/°C with a positive temperature coefficient. However negative temperature coefficient can be achieved by reversing the diode polarity and associated bias circuit. An important observation in the above circuit is that point X_1 is going to vary linearly over temperature.

Desired value of the temperature correction at the inverting mode of A_2 can be achieved by using a scale down resistor in series with the point X_1.

Results of A_1

AC gain check over temperature

Power Supplies +5.998 VDC

-6.004 VDC

Power supplies were constantly monitored and kept constant to simulate built in regulators.

Temp	Time	Input	Output	Gain
25°C	9.15 am	10 mv	500 mv	50
-54°C	10.50 am	10 mv	500 mv	50
75°C	1.30 pm	10 mv	495 mv	49.5

As can be seen, enough stabilization time was allowed at each temperature for the unit under test.

DC Offset Check

Test Circuit

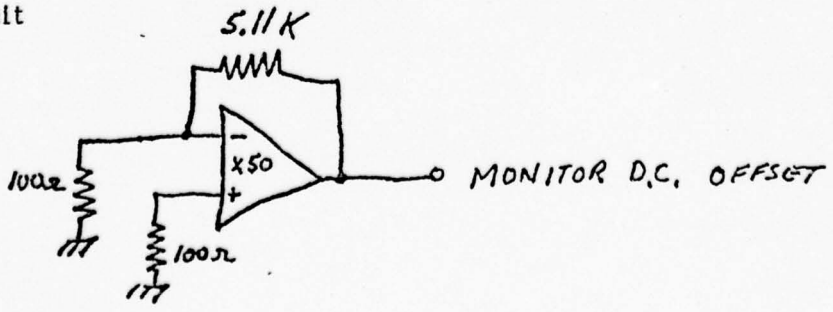


FIG. 15

Note: Power supplies were constantly monitored and kept constant to simulate built in regulators. 45 minutes were allowed per temperature for stabilization.

Temp

Desired	Actual	Output DC Offset
-54°C	-54°C	-13.30 mv
-25°C	-28°C	-14.05 mv
0°C	-1°C	-15.09 mv
25°C	24°C	-15.85 mv
	Unit @ 24°C overnight	
25°C	28°C	-15.45 mv
75°C	75°C	-16.70 mv

Observation of the above data indicates that:

Output drift from 28°C to 75°C _____ 26.59 μv/°C

Input drift from 28°C to 75°C _____ 0.43 μv/°C

Output drift from 28°C to -54°C _____ 26.2 μv/°C

Input drift from 28°C to -54°C _____ 0.52 μv/°C

The above results meet design objectives quite satisfactorily.

Results of A_2

More than two cycles were repeated at random to check the repeatability. Each reading was recorded after about 45 minutes of stabilization time.

TEMPERATURE		OUTPUT DC OFFSET
Designed	Actual	
25°C	23°C	56 mv
-25°C	-27.5°C	24 mv
-50°C	-54.5°C	6.2 mv
-25°C	-28°C	20.2 mv
+50°C	+51.5°C	77.2 mv
+75°C	+75°C	97.5 mv
+50°C	+47°C	78.0 mv
-25°C	-28°C	22.1 mv
+25°C	+30.5°C	56.8 mv

The average drift refered to the input is about 65 μv/°C and linearity is quite satisfactory.

Results of A_3

Actual temperatures same as for A_2

output voltage (mv)

1. -5.24
2. −212.0
3. -351.4
4. -247
5. +114.8
6. +215.2
7. -1116.3
8. -228.6
9. +28.0

Computed mv/°C for the successive readings are:

1. 4.09
2. 5.16
3. 3.93
4. 4.55
5. 4.27
6. Improper circuit operation
7. " " "
8. 4.38

It is obvious from the above data that there was some malfunction in the circuit. The experiment was repeated after changing the devices and achieved results were very satisfactory. Average drift was 4.1 mv/°C.

Next is was decided to cascade A_1 and A_2 (Net gain = 500; 54.0 dB) and run the combination over temperature. Purpose was to find out the value and linearity

of the overall offset drift so that temperature compensation from the diode/741 circuit can be computed. Results for two complete cycles are given below.

Temperature (°C)		
Desired	Actual	Output offset (mv)
-50	-55	236
-25	-29	204
+25	+27	131
+50	+52.5	95
+75	77.5	64
+50	52.5	95
+25	24.5	134
-25	-29	210
-50	-55.5	242

Computed output drift in mv/°C between two successive data points is:

1. 1.2
2. 1.3
3. 1.41
4. 1.24
5. 1.24
6. 1.39
7. 1.42
8. 1.2

Since drift was not very linear and repeatable it was decided not to try to temperature compensate the amplifier. It should be pointed out that any temperature variation can be achieved from the temperature compensation circuit, but it has to be linear. However, since A_1 (X 50 amplifier with high loop gain and overall feedback) had quite low and linear drift, it was decided to cascade two amplifiers of this type to get most of the gain. Due to the negative swing requirement, a unity gain amplifier was also included. This approach was preferred despite of the additional circuitry

as a moderate but linear output offset drift was expected.

Block diagram is shown below.

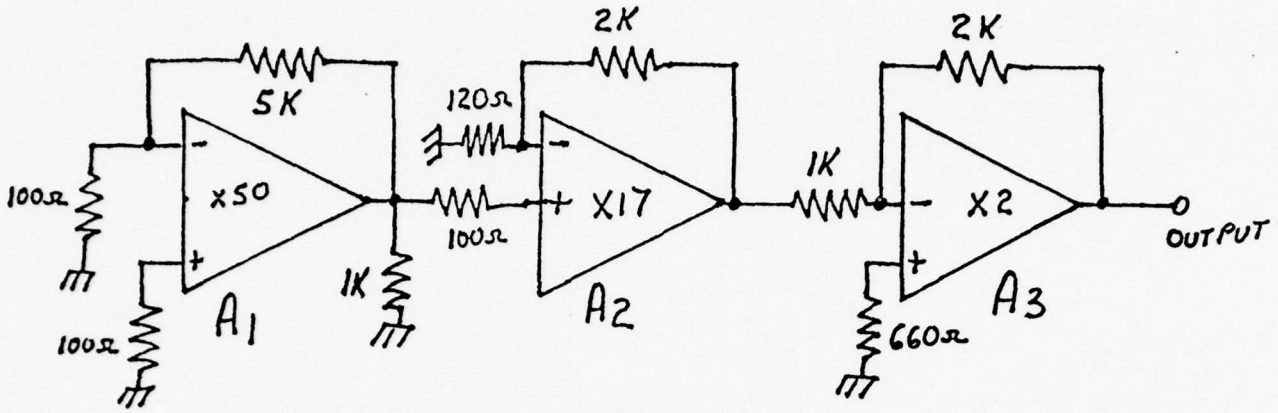


FIG. 16

A_3 is the one differential pair type described earlier. A fixed AC signal was applied at the input to find out the AC gain change over temperature.

Results are:

Temperature (°C)	dC offset (mv)	AC output (mv)
-50	82	-230
-25	19	-233
0	+6.9	-240
+25	0	-250
+50	0	-245
-50	61	-245
-25	13.5	-250
0	-11.6	-241
25	- 6.5	-234
+50	0	-228

It is clear from the above data that results are not in line with the design objectives. On isolating the amplifiers and rerunning the experiement, it was found that A_2 was malfunctionting. All devices were changed in A_2 and the whole combination was re-run over temperature. Output drift was on the order of 1.2 mv/°C and was fairly linear.

Breadboard of Detector Log Amplifier

After achieving satisfactory results with high gain linear amplifier, it was decided to breadboard a detector log amplifier. Tunnel diode detector was used for simulation purpose. It should be pointed out that very nearly equal D.C. offset drift will be generated by the temperature compensation circuit described earlier and applied on the non signal transistor of the log differential pair. In this way most of the D.C. offset drift from the high gain amplifiers will be rejected as common mode signal by the differential pair. Block diagram of the approach is shown below.

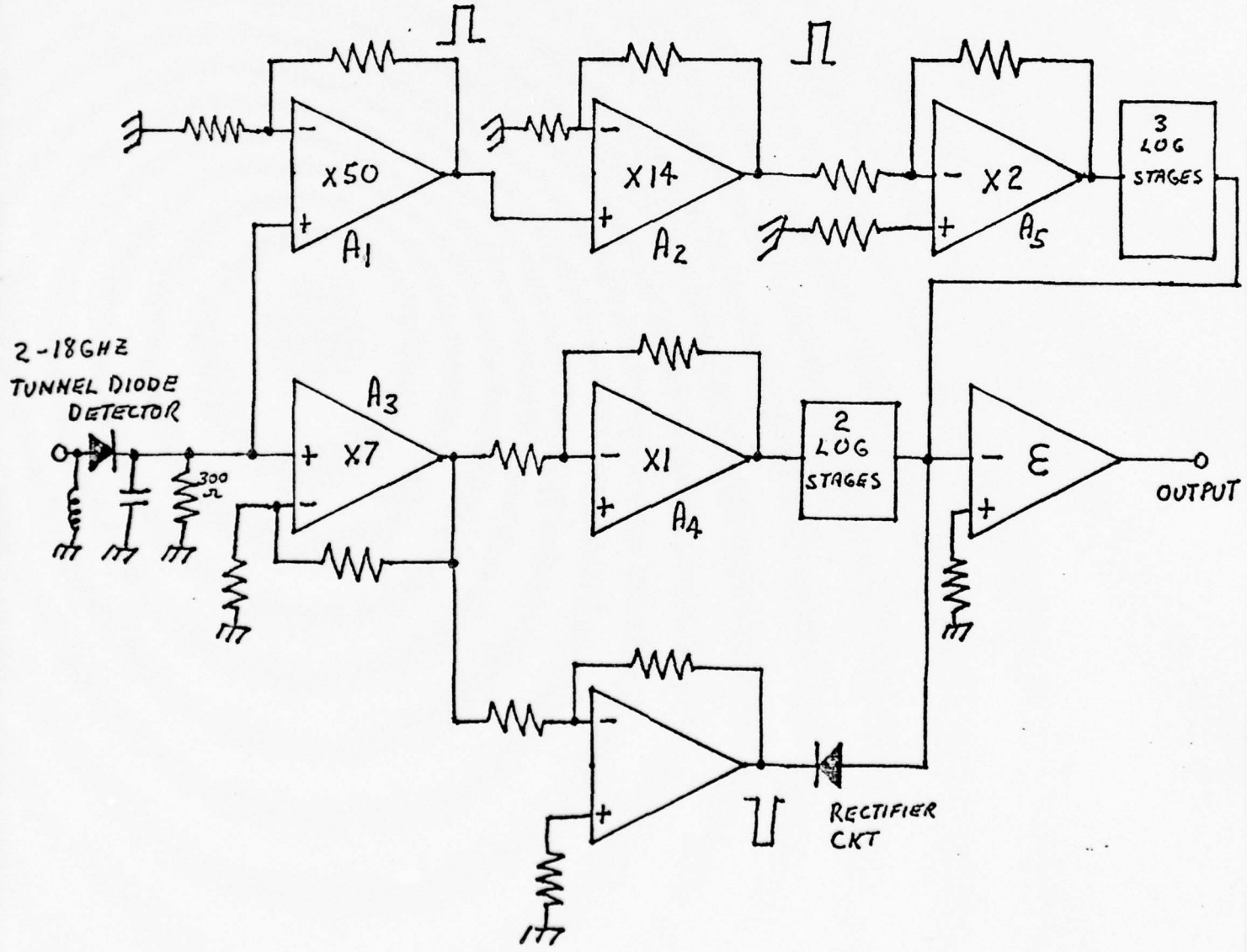


FIG. 17

** Standard 741 type circuit for bias

Standard 741 type temperature

Compensation and built in power supply regulators

Unit was aligned at room temperature at 10.0 GHz and the results are shown in the attached graph paper.

Temperature Performance

First run of the unit over temperature gave very unsatisfactory results. Detector, linear amplifiers were then separated from the logging stages and rerun over temperature. This change still produced nonlinear and significiant D.C. offsets.

After this step detector in combination with A_1 only was taken over temperature. This block gave very satisfactory results and were similar to the results achieved earlier on the A_1 amplifier in linearity and magnitude of the DC offset drift.

Analysis of the various temperature runs indicated that possible problems were due to the interaction between the amplifiers A_1, A_3 and detector, as both A_1 and A_3 were simultaneously loading the tunnel diode detector. Inorder to avoid interaction problems, a new approach was configured. This would include only putting one amplifier on the detector. The output of the amplifier (gain = 7) can provide current drive (sourcing as well as sinking capability) and also offer extremely low AC and DC source impedance. Block diagram of the approach is shown in figure 18.

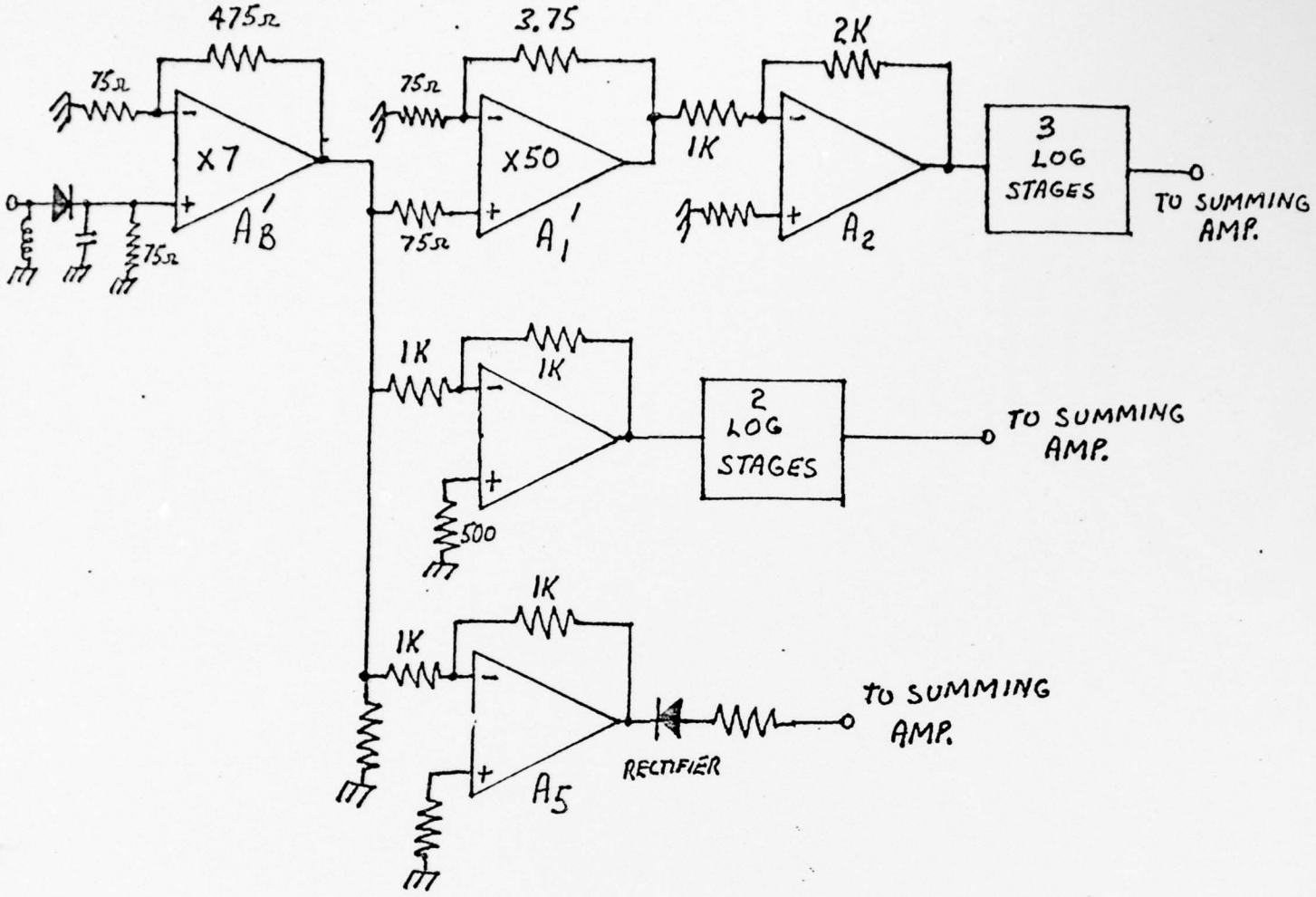


FIG. 18

Above circuit was breadboard and run over temperature. I should be pointed out that about 30 minutes stabilization time was allowed for each temperature. Results are given below. Table indicated DC offsets. Temperature compensation will be applied to the non signal transistor of the differential pair fed from A_2.

Temperature	A_1	A_2	A_3	A_4
	(mv)	(mv)	(mv)	(mv)
-53.5	347.4	72	7.24	70
+35	366.2	43.5	7.27	77.9
+73	385	+9	8.2	81.7
+35	368.3	+40	7.8	77.98
73.5	386	7.8	8.22	81.9

Unit was aligned at room temperature and appropriate temperature compensation applied to the first log stage. Recorded at @ 10.0 GHz for the detector log amplifier is given below.

Input RF Power (dBm)	Output AC Amplitude (mv)			Output DC offset		
	-54°C	25°C	75°C	-54°C	25°C	75°C
-41	75	65	65	340	280	290
-40	87	80	78			
-35	180	200	180			
-30	288	310	293			
-25	410	440	425			
-20	555	585	560			
-15	665	730	720			
-10	780	865	870			
- 5	920	1030	1050			
0	1090	1180	1170			

Input RF Power	Output Peak Value (AC amplitude + DC offset)		
	-54°C	25°C	75°C
-41	415	345	355
-40	427	360	368
-35	520	480	470
-30	628	590	583
-25	750	720	715
-20	895	865	850
-15	1005	1010	1010
-10	1120	1145	1160
- 5	1270	1310	1340
0	1430	1460	1460

Results show $\lesssim \pm$ 1.0 dB error from -30 dBm to 0 dBm. Since compensation was not competely right, error from -40 dBm to -30 dBm was about -2.5 dB. The main emphasis in the experiment was to check the concept of applying the temperature compensation and therefore the unit was not re-compensated.

In order to make certain that reconfiguration was a solid and repeatable design, it was decided to breadboard two identical units as blocked below.

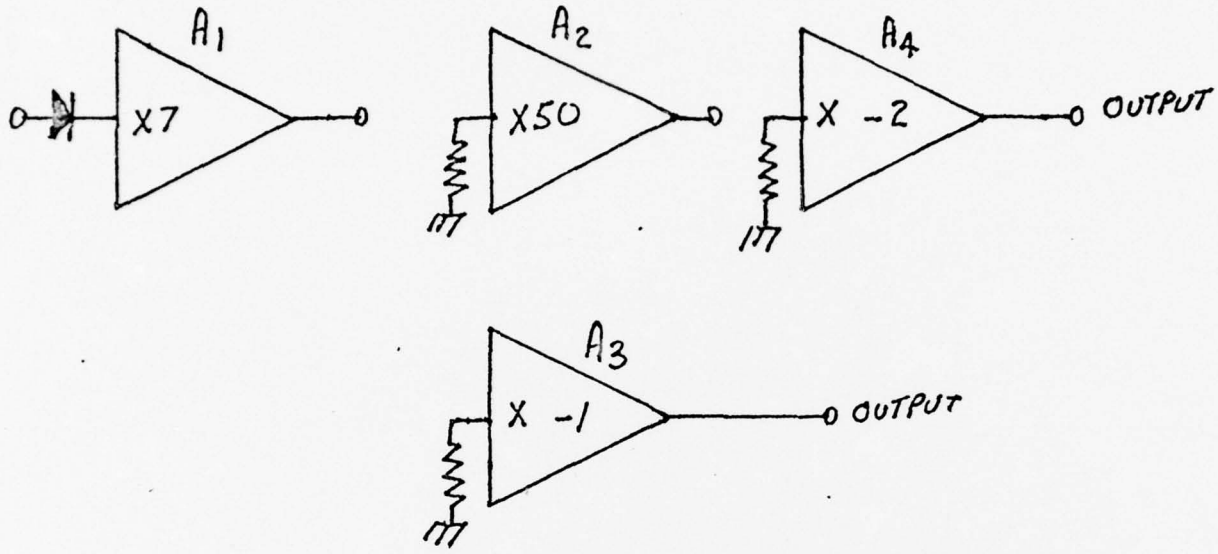


FIG. 19

Results achieved are given below:

Temp	Unit 1				Unit 2			
°C	A_1 mv	A_2 mv	A_3 mv	A_4 mv	A_1 mv	A_2 mv	A_3 mv	A_4 mv
-50	-5.2		1.7	4.8	-4.75	-12.7	15.4	29.3
-25	-5.0		6.9	13.0	-4.52	-12.9	19.8	36.6
+24	-4.5		15.7	27.2	-4.06	-15.3	29.8	52.3
+70	-4.1		27.1	45.3	-3.6	-14.8	40.8	69.7
-50	-5.3		2.0	5.0	-4.74	-12.5	15.4	30
-25	-5.0		6.6	12.9	-4.55	-13.7	19.4	36.3
+25	-4.5		17.1	29.3	-3.93	-15.0	32.1	56.1
+70	-4.1		27.1	45.2	-3.6	-14.7	40.9	70.0
-50	-5.2		2.2	5.1	-4.74	-12.3	15.6	30
-25	-5.0		6.1	11.3	-4.56	-13.3	19.2	35.9
+25	-4.5		16.2	27.5	-4.05	-15.4	29.6	52.1
+70	-4.1		27.5	45.3	-3.6	-14.9	41.0	70.0

As it is clear from the above results, that they are quite satisfactory.

5.0 QUARTERLY PROGRESS REPORT

This covers the period ending February 28, 1974, as follows.

QUARTERLY PROGRESS REPORT

(period ending Feb. 28, 1974)

prepared for

U.S. Naval Research Laboratory

Washington, D. C. 20375

Contract No. N00014-74-C-0020
Req'n No. 00173-3-006371/2-27-73

prepared by

Aertech Industries

825 Stewart Drive

Sunnyvale, California 94086

1. INTRODUCTION:

Since the last reporting period the interdigitated design of the low frequency coupler was terminated because the design approach taken did not respond to changes and acted more like an octave coupler rather than provide performance over the 102% fractional bandwidth that is required. Therefore, the design has been redirected towards a four diode single ended type of detector. For the high frequency circuit the coupler provides adequate performance so that a balanced configuration is being pursued.

In the field of amplifier hybridization of the first portion of the logging amplifier has been screened, fired, packaged and tested. The second portion is ready for screening and firing.

In the area of packaging a new parallel seam sealer has been purchased that will be capable of sealing the dual inline packages that house the amplifier circuits.

2. LOW FREQUENCY DETECTOR:

The current design for the low frequency detector consists of a single ended design using four beamlead schottky barrier detector diodes in video series and RF parallel. This type of circuit provides a higher output voltage because the four diodes are in video

series and also provides a lower RF diode impedance because the diodes are in RF parallel. A four diode single ended detector has been fabricated on a chrome gold metalized ceramic circuit. Figure 1 is a copy of the artwork with the components shown in place. Testing is under way to determine its potential. Some preliminary data tken has shown K values of 2500. More data is due to be taken to evaluate the potential of this configuration.

One of the difficult design areas that will be closely observed will be the relationship of input VSWR with power level. Although, the circuit by biasing may achieve good VSWR at low input power levels, it is not yet known that it will maintain a good VSWR at the higher power levels. For the next reporting period data will be available on this detector configuration and should show if it will meet all intended design goals.

3. HIGH FREQUENCY DETECTOR:

The circuit design for the higher frequency consists of a balanced design utilizing an interdigitated 3 dB coupler with the isolated port terminated in 50 Ω and utilizing beamlead Schottky barrier diodes in video series. This design approach provides a better input VSWR over the single ended designs because reflections from the diodes are absorbed in the 50 load on the coupler isolated port. The coupler used is the same coupler described in the previous report except that the gap width between interdigitated lines is 0.3 mils wide. The

SK080

SCALE 10:1

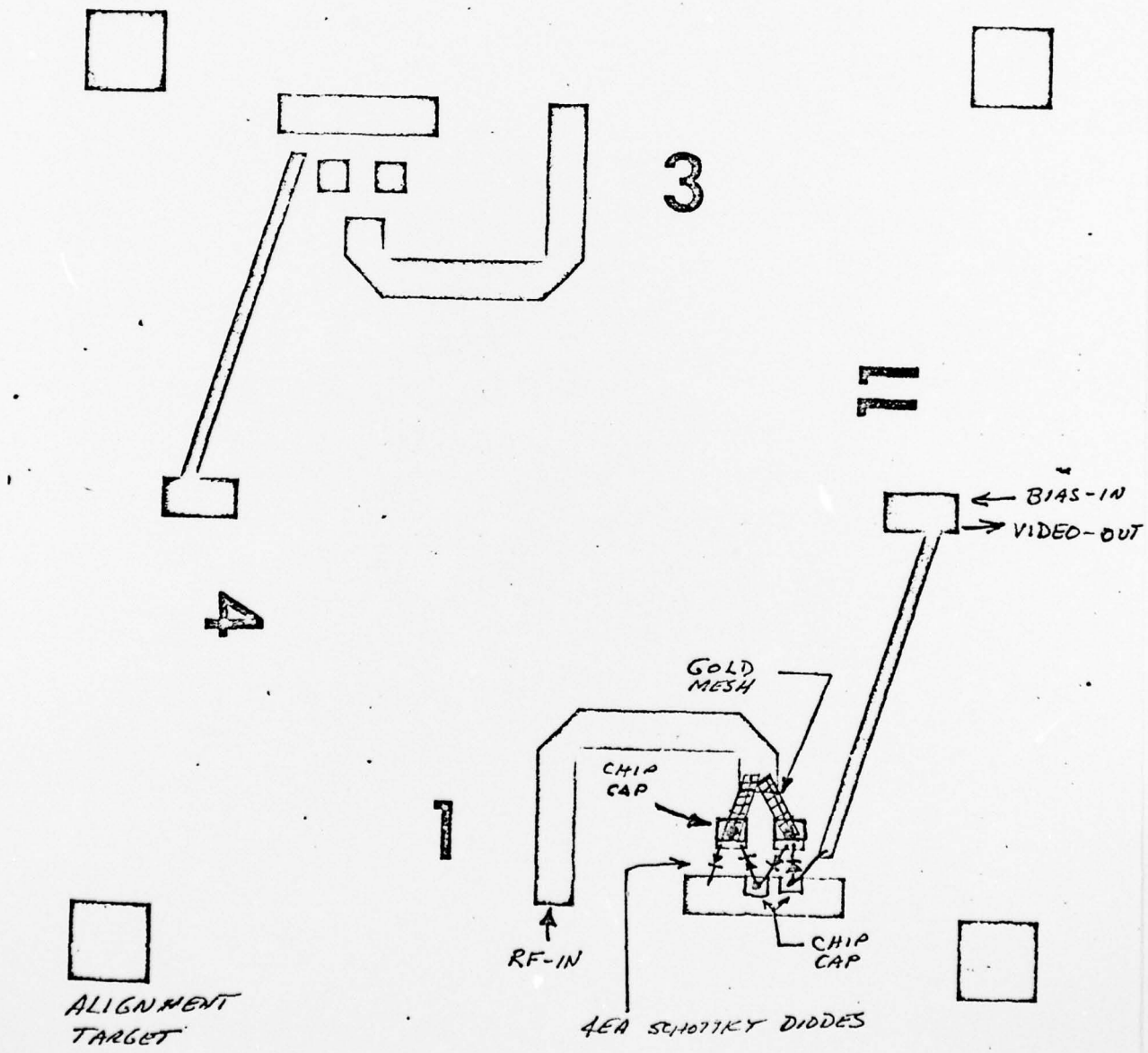


FIGURE 1

LOW-FREQ DETECTOR CIRCUIT :

reason for narrowing the gap spacing is to allow for the etch factor when etching this circuit. Nominal gap widths after etch are approximately 0.7 to 0.8 mil. This coupler provides adequate performance over the required frequency range.

Two circuits for this frequency were fabricated. Figures 2 and 3 are copies of the artwork with components in place used for these circuits. The two circuits are almost identical except that circuit # 2 has a series of narrow lines for the purpose of varying the impedance of the connectin glines and the diodes. The circuit in Figure 2 has a single 60 ohm line going into the diode with some tuning pads along the line length to assist in tuning the circuit. The diodes use an etched bypass capacitor for each diode. A 2pF beamlead blocking capacitor was required for the purpose of providing D.C. isolation during biasing.

Preliminary data has been taken on both circuits. The data show that both circuits act almost identically. The untuned circuit has a minimum output voltage of 15 millivolts (one frequency only) and the maximum VSWR with 50 microamps of bias a 1 meg ohm load and an RF input of -20 dBm is 2.5:1. When looking into a 2K load the minimum voltage drops to 8 millivolts and the VSWR remains the same. The output voltage is not smooth since the highest area has over 25 millivolts of output which shows that the circuit needs tuning. The VSWR is improved to 2 to 1 by increasing the bias to 300 microamps

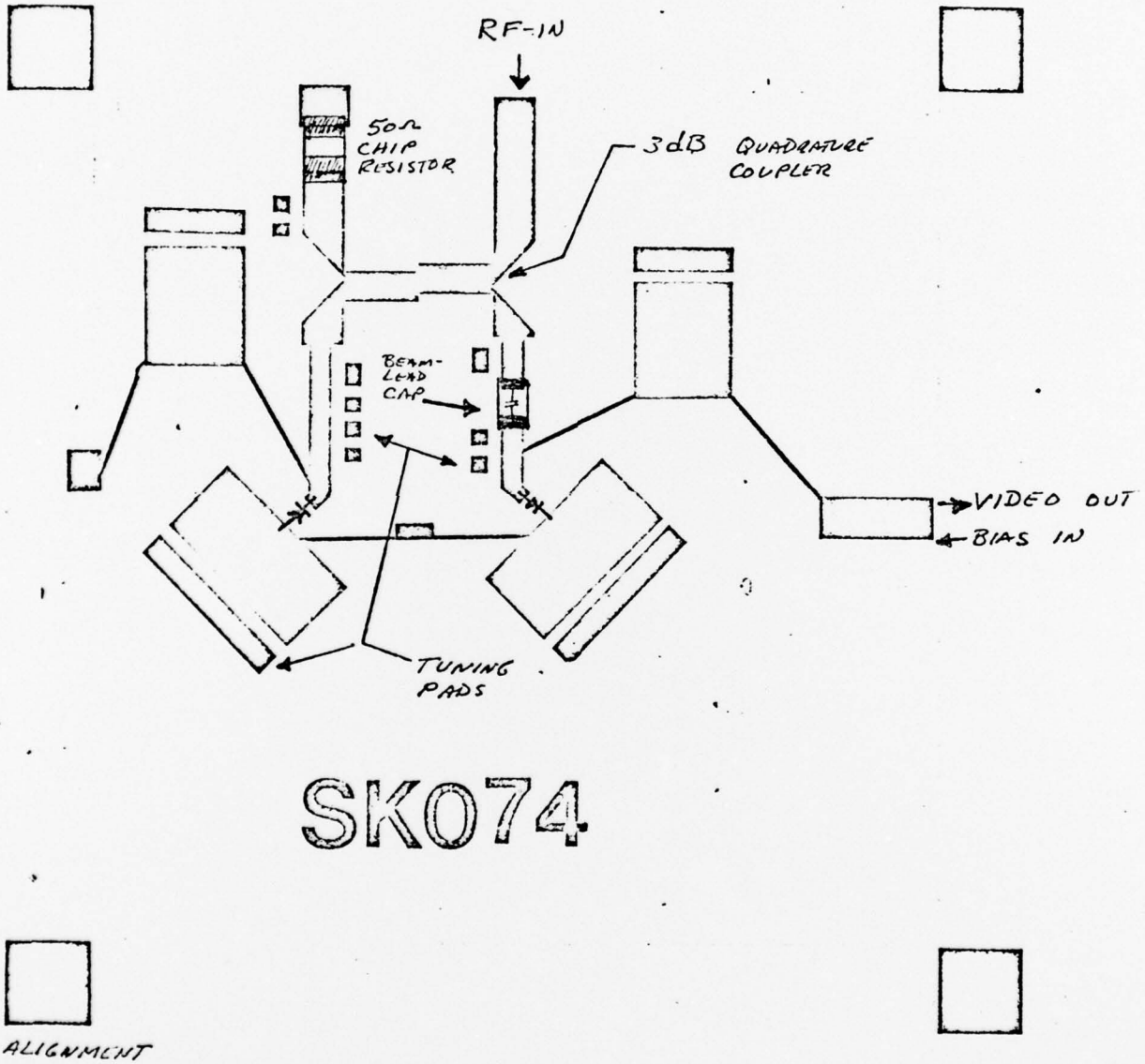


FIGURE 2.

HIGH-FREQ DETECTOR CIRCUIT

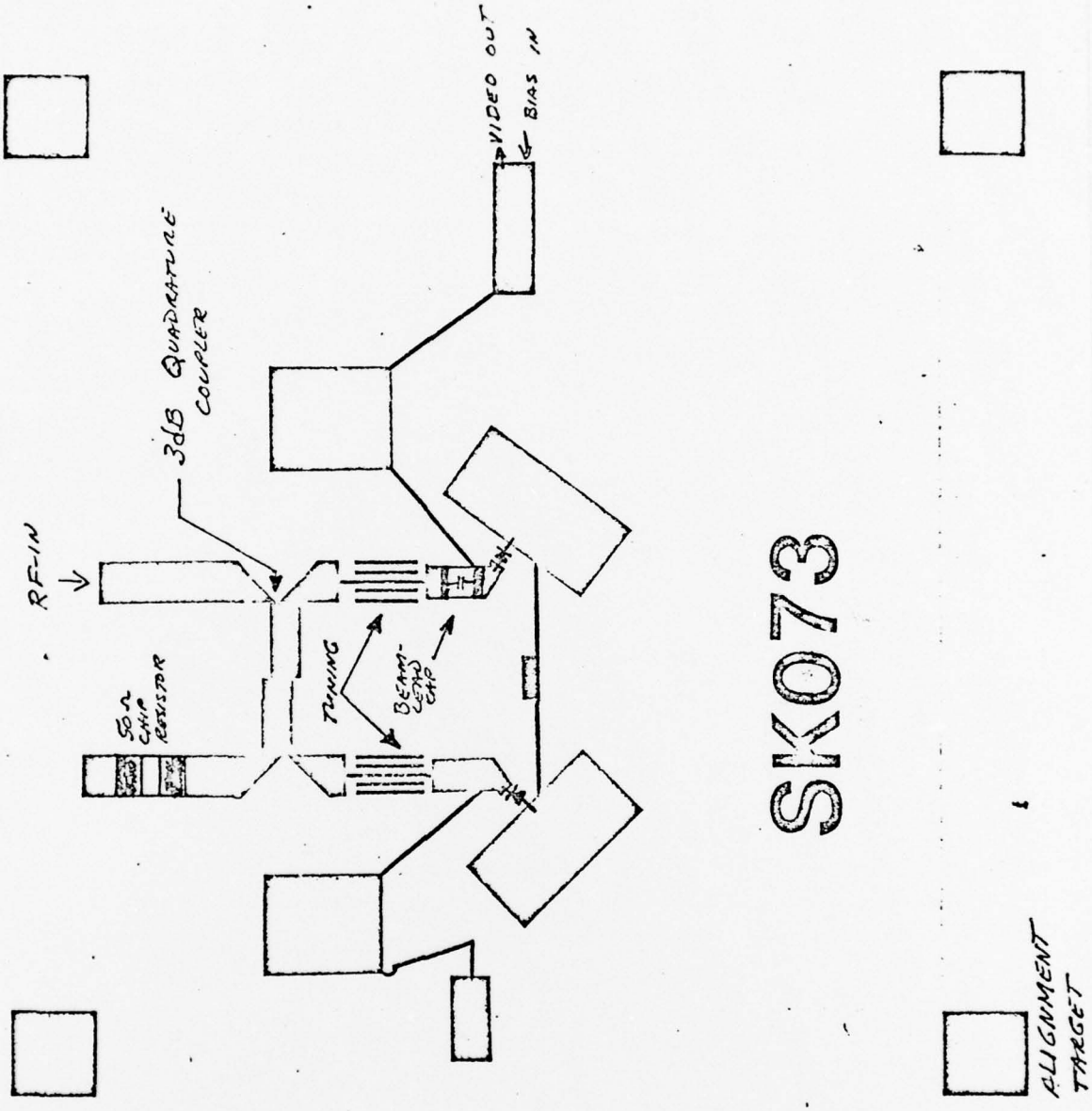


FIGURE 3

HIGH-FREQ DETECTOR CIRCUIT

and the output voltage minimum remains the same but the overall output smooths out significantly. Work is in progress to tune the circuit to achieve its maximum potential. For the next reporting a tuned circuit technique will be arrived at, and the modification will be incorporated into a new circuit.

4. AMPLIFIER HYBRIZATION:

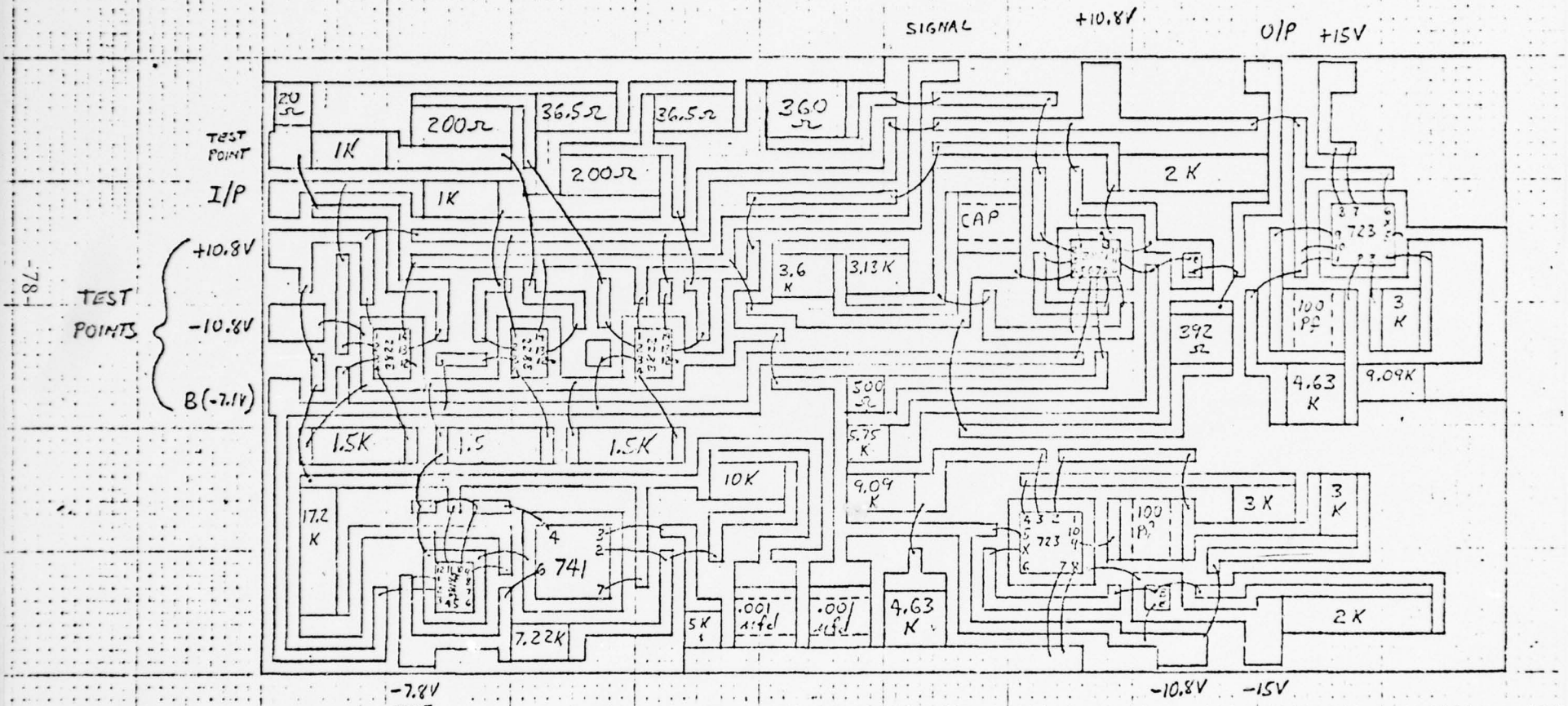
The first layout consisting of the three logging stages and power supply was redone to fit in a 0.5 x 1.00 x 0.025 inch substrate. This circuit has been screened and fired and fabricated. The chip transistor arrays were silver epoxied to the substrates and the wire connection were made by ultrasonic bonding machine using 1 mil diameter aluminum wire. A total of over 100 bonds were made on this single substrate. Figure 4 shows the top assembly configuration of this circuit. The substrate was packaged in a 24 pin dual in-line package with the appropriate circuit input and output carried through designated pins in the package. Testing of this circuit will be reported in the amplifier portion of this report.

The second circuit, a video amplifier, has been reduced to artwork form and transferred to screens but this circuit has not yet been screened and fired on a ceramic substrate. Figure 5 is a Top Assembly view of the second circuit.

FIGURE 4

SK032-

LOG AMPLIFIER TOP ASSEMBLY



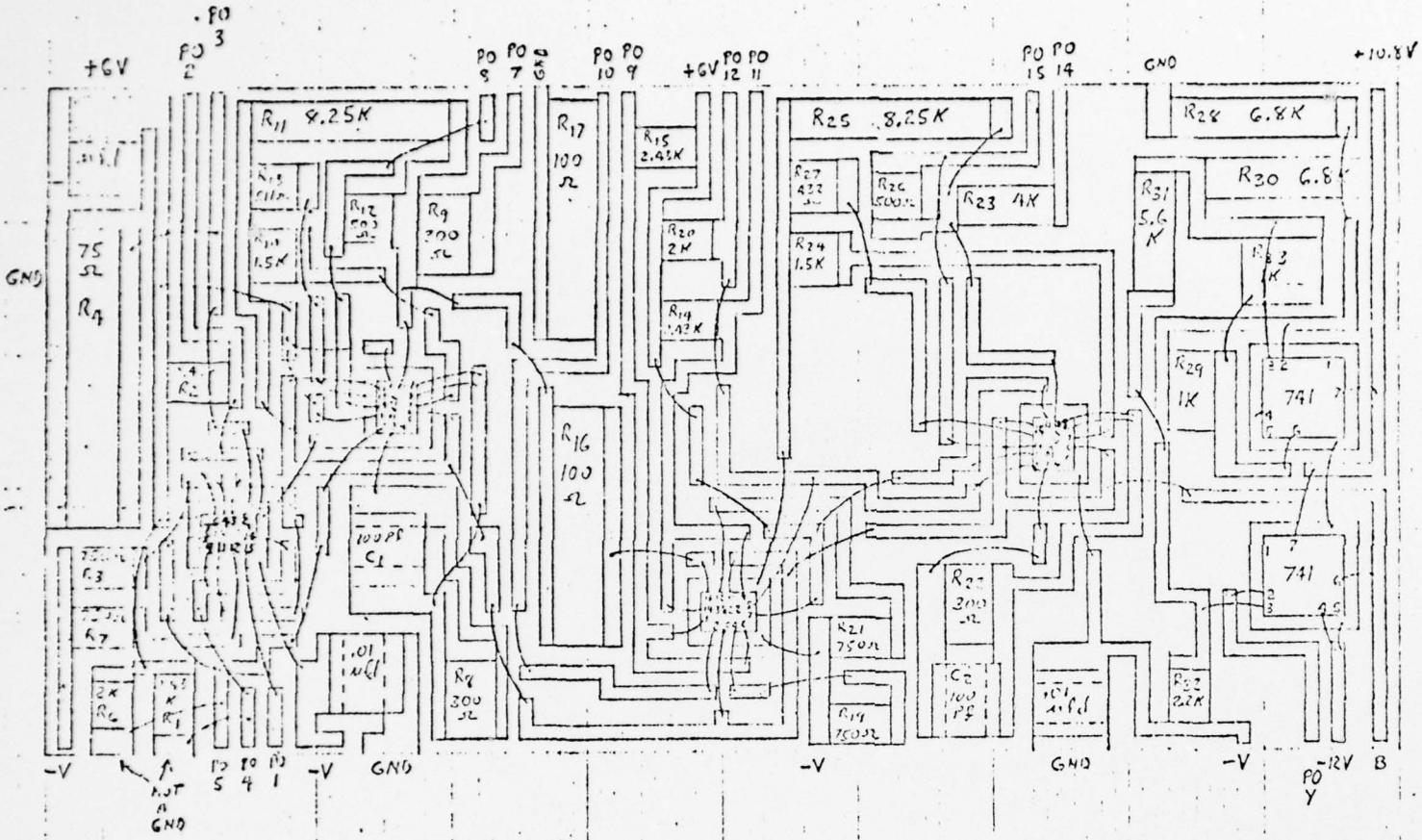


FIGURE 5

SK063 AMPLIFIER TOP ASSY

5. TECHNIQUES:

During this reporting period progress has been made in the area of thin film and thick film and thick film processes. Specifically in the thin film processes the etching times have been reduced by changing the etchants and also the viscosity of the photo resist. By increasing the viscosity of the photo resist the circuit configuration breakdowns have been reduced. The chrome etch has been changed to a potassium ferricynaide solution and the gold etch is now a commercial type (C-35) made by Film Microelectronics Incorporated and is used at an elevated temperature. The exposure and developing time has been also changed to compensate the change in photo resist viscosity. This faster rate of etching eleminates some of the undercutting of the gold or chrome in the circuits. The etching is now more consistent and the etch factor has been reduced to approximately 0.3 mils.

In this thick film area better mask control has been achieved by providing a more precise method of mask aligning. This provides a method for step and repeating processes i.e., different resistor inks without misalignment of the resistor patterns. This provides a faster method of printing of high density circuits such as these. Additionally, the resistor abrasive trimmer has been improved to make a smoother working machine and also providing the operator a more positive control. This will provide a capability for trimming circuits with high density resistor patterns.

Some work is being done using precoated screens, that is buying a screen that has an emulsion thickness of known value. The emulsion thickness is very improtant in printing good circuits since the thickness of the resistor ink determines the value of the resistor. By purchasing screens with uniform emulsion thickness, operator error in making screens is substantially reduced. For the next reporting period Aertech's goal is to have a much quicker and easier method for producing thick film circuits.